INVESTIGATION OF A MULTI-GHz SINGLE-CHIP CMOS PLL FREQUENCY SYNTHESIZER FOR WIRELESS APPLICATIONS

BY

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In this dissertation, the feasibility of implementing an integrated Phase-Locked Loop (PLL) CMOS Frequency Synthesizer (FS) is discussed. The most challenging part in the loop is the integrated Voltage-Controlled Oscillator (VCO). To achieve low phase noise, the quality factor (Q) of an on-chip resonator consisting of inductors, varactors and transistor parasitics must be improved. Through a layout optimization, Q of >140 at 5.5 GHz and >40 at 26 GHz for MOS capacitors have been achieved. Q of 57 at 5.5 GHz for a pn-junction diode which is sufficient for varactor applications has been measured while Q of 57 at 1.1 GHz for transistor parasitics has also been achieved.

A modified negative-resistance oscillator topology which utilizes only PMOS transistors is developed. Using this oscillator topology for a 1.24-GHz VCO, phase noise of -137 dBc/Hz at a 3-MHz offset which meets the Global System for Mobile Communications (GSM) requirement has been measured.

Additionally, by using an inductor structure incorporating a spiral inductor and package parasitics, a 1.1-GHz 13-mW VCO with extrapolated phase noise of -140 dBc/Hz at a 3-MHz offset is demonstrated. These phase noise results are the lowest reported to date for 1-GHz single-stage CMOS VCOs. To improve the power supply rejection ratio for the modified VCO topology, a bias circuit has been designed and integrated with 5.5-GHz VCOs. Phase noise of these integrated VCOs is -117 dBc/Hz at a 1-MHz offset which is the lowest phase noise reported to date for 5.5-GHz CMOS VCOs. To investigate the capability of CMOS technologies, an LC oscillator operating at 25.9 GHz is also demonstrated in a partially scaled 0.1-μm bulk CMOS process. Currently, the 25.9-GHz VCO is the CMOS circuit with the highest operating frequency.

Finally, an integrated 5.5-GHz PLL FS implemented in a 0.25-μm CMOS process is demonstrated. To reduce switching noise, the prescaler is designed using a source-coupled-logic structure. The prescaler has a fixed division ratio of 128 and consumes only 4.1 mW at 5.4 GHz. A new charge pump circuit is developed to reduce the current glitch at the output node while maintaining a sufficient switching speed. By incorporating a voltage doubler and level shift circuits with the charge pump, the VCO input voltage range is increased from 1.3 to 2.5 V with immeasurable phase noise degradation to the PLL. The phase noise of the FS is lower than that of the free running VCO by >50 dB at a 1-kHz offset, and the spurs are >63 dB below the carrier. The experimental results suggest that a CMOS FS operating above 5.5 GHz with adequate performance for high-bit-rate applications is feasible.

CHAPTER 1
INTRODUCTION

With the explosive growth of the wireless communication industry, communication circuits research has received great attention. The major issues being addressed are low voltage, low power and low cost designs which achieve necessary performance. The radio frequency (RF) front end circuits have been implemented with Gallium Arsenide (GaAs) MESFET, Si-bipolar junction transistors (BJTs), III-V heterojunction bipolar junction transistors (HBTs) and Si-Germanium (SiGe) BJTs while the baseband digital signal processing (DSP) and analog circuits are being implemented exclusively using CMOS technologies. As the focus of the wireless communication industry moves toward the personal communication system (PCS) and wireless local area networks (WLANs) as well as the wireless entertainment electronics, light, small-dimension, low-cost, low-power and a higher level of integration are becoming ever critical. These have intensified the interests in low cost CMOS technologies due to their low cost, high yield and higher level of integration including baseband circuits.

As the feature size of the CMOS technology becomes smaller, the frequency at which CMOS transistors can operate while delivering acceptable performance becomes higher. Several work [1], [2] has shown the feasibility of

CMOS front-end circuits and the performance gap between the CMOS and BJT circuits has been narrowing [3]. The ultimate goal for the wireless industry using CMOS process technology is to take the advantage of the CMOS process to implement an inexpensive single chip radio including an RF front end, intermediate-frequency (IF) modulation/demodulation (modem) circuits and baseband signal processing circuits.

1.1 An Overview of an RF Transceiver

Figure 1-1(a) shows a general block diagram of a radio [4]. In the receive mode, the RF signal is received by the antenna and filtered by the duplexer to attenuate the transmit band signals. The filtered signal is amplified by a low noise amplifier (LNA) followed by an RF filter (image rejection filter [5]). The RF filter is used to keep the unwanted frequency components from being fed into the RF mixer in order to reduce the unwanted signal at the mixer output. The RF mixer downconverts the RF signal to IF using the LO generated by the frequency synthesizer. The IF signal is then demodulated by the I/Q demodulator which outputs in-phase and quadrature-phase data for a digital signal processor to reconstruct the message. The requirement of the GSM receiver is that a -102 dBm signal power with 9 dB of signal to noise ratio (SNR) at the input of a receiver must be detected with a bit error probability (BER) $< 10^{-4}$. The system must also be able to reject a 0-dBm out-of-band single-tone blocking signal, a -23-dBm in-band single-tone blocking signal and -43-dBm in-band two-tone blocking signals. These impose stringent

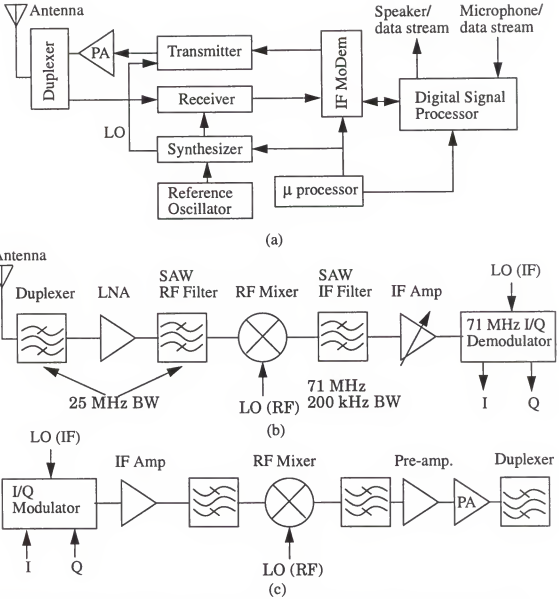


Figure 1-1 (a): A general block diagram of a cellular radio. (b): A typical receive path. (c): A typical transmit path.

requirements on the RF LO. Figure 1-2 [6] illustrates the effect of LO purity in a receiver. Since the wanted signal power is small and the interferer is large, the noise (skirt) of the LO must be low so that the wanted signal would not be corrupted after the downconversion.

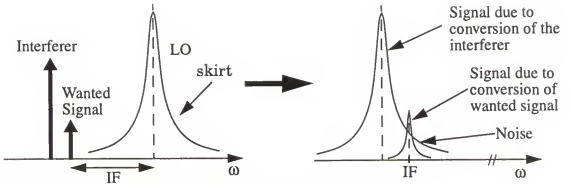


Figure 1-2 The effect of LO phase noise in a receiver.

In the transmit mode, the input message is first processed by the digital signal processor to generate in-phase and quadrature-phase data streams. The data streams are then modulated with IF LOs (in-phase and quadrature-phase) followed by an IF filter. The IF signal is mixed with an RF LO which is again generated by the frequency synthesizer. Finally, the RF signal is filtered and amplified by a power amplifier (PA), and is fed to the antenna through a duplexer which attenuates the spurious signal level. One of the key requirements for a transmitter in a wireless communication system is to provide a good modulation accuracy in order to minimize the BER of the communication link as well as the BER of other systems operating nearby through a reduction of the unwanted sidebands, LO leakage, and spur products caused by intermodulation. The spurious transmitted noise power falling into the receive band could degrade the performance of nearby receivers and could even corrupt the signal (Figure 1-3 [6]). This once again leads to a challenging noise requirement for the noise skirt of the RF LO. The tough standards for modern wireless communication systems result in very tight specifications on the close-in and far-out phase noise of synthesizers [6].

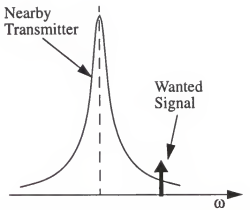


Figure 1-3 The effects of LO phase noise in a transmitter.

There are many frequency synthesizer architectures. Shown in Figure 1-4 is a general block diagram of an integer-N phase-locked loop (PLL) frequency synthesizer [7], [8]. The output is directly connected from the voltage-controlled oscillator (VCO) which generates the signal at the desired frequency. A dual modulus prescaler divides the output of the VCO (f_{VCO}) by N or (N+1). The prescaler divide ratio is controlled by the programmable A/B counters. If counter A is active, the prescaler divides f_{VCO} by N. Otherwise, it divides f_{VCO} by (N+1). After finishing count-down of the values in counters A and B, which are set by the digital control word, the programmable A/B counter block outputs a pulse to phase/frequency detector (PFD). This pulse train (f_{div}) from the A/B counter is then compared with a reference frequency (f_{ref}). The reference frequency is usually generated by a temperature compensated crystal oscillator (TCXO) and has very low phase noise. The PFD is a finite state machine. If the f_{div} falls before f_{ref} falls, the signal DN is high. If f_{div} falls after f_{ref} falls, UP is high. If f_{ref} and f_{div} fall simultaneously, then both

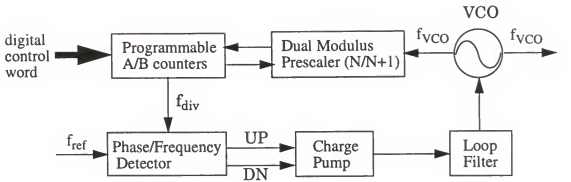


Figure 1-4 A general block diagram of an integer-N phase-locked loop (PLL) frequency synthesizer.

UP and DN remain low. The UP and DN signals control a charge pump (CP) to source a current to the loop filter (UP=1) or to sink a current from the loop filter (DN=1). The output of the loop filter is then fed back to the VCO to control the frequency. The loop is in the "lock" condition if and only if f_{ref} and f_{div} have the same phase and frequency. Otherwise, the loop will adjust itself until the lock condition is reached. The relationship between f_{ref} and f_{VCO} is

$$f_{VCO} = f_{ref} \cdot (A \cdot N + B \cdot (N + 1)) \qquad (1.1)$$

The phase error between f_{div} and f_{ref} resulting from the phase noise of the VCO is translated to a voltage difference by the PFD, CP and loop filter, and is then fed back to VCO input to compensate the phase change at the VCO output. The transfer function of a PLL is typically a low-pass-filter function and is determined by all components in the loop. If the phase change of the VCO is slow, the phase error between f_{div} and f_{ref} would vary slowly and the voltage difference could be passed to the VCO input. If the phase of the VCO

changes rapidly, the phase error and thus the voltage difference would be attenuated by the low pass characteristic, and the VCO output would not be adjusted. Hence, the phase noise of the frequency synthesizer within the loop bandwidth can be reduced and excellent phase noise performance is possible (Figure 1-5). Since the loop bandwidth of a PLL also determines the loop dynamics such as acquisition time, it is typically designed according to intended applications.

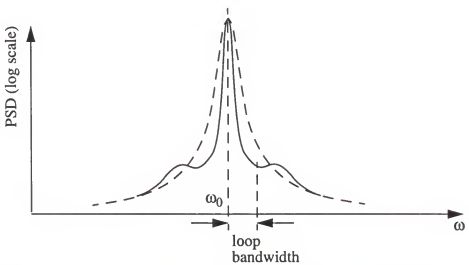
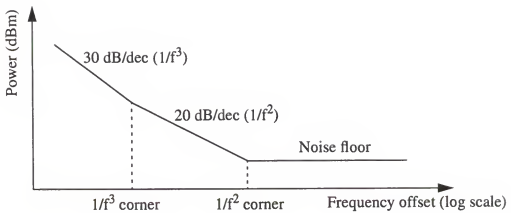


Figure 1-5 A free running VCO output spectrum (dashed line) and a typically PLL output spectrum (solid line).

The most challenging part in the loop is the integrated VCO. It directly determines the phase noise of the output signal (f_{VCO}) outside the loop bandwidth. The first difficulty is achieving low phase noise at small frequency offsets from the resonant frequency using CMOS technology which has high 1/f noise due to traps and defects in the oxide and oxide silicon interface. This results in high phase noise in the $1/f^3$ region (Figure 1-6) of a VCO output



$$\mathcal{L}(\Delta\omega) = 10 \cdot \log\left\{\frac{2FkT}{P_s} \cdot \left[1 + \left(\frac{\omega_0}{2Q \cdot \Delta\omega}\right)^2\right] \cdot \left(1 + \frac{\omega_{1/f^3}}{|\Delta\omega|}\right)\right\}$$

Figure 1-6 A typical VCO phase noise plot.

spectrum. The second difficulty is the limited Q of on-chip passive components. This leads to large power consumption and poor phase noise performance. The equation (known as Leeson's model [9]) in Figure 1-6 depicts the typical VCO sideband and the relation between tank Q and phase noise where F is the noise factor of the active device(s) inside a VCO, k is the Boltzmann's constant, T is the temperature, P_s is the signal power, Q is the overall tank Q, ω_0 is the resonant frequency, $\Delta\omega$ is the frequency offset from the carrier, and ω_{1/f^3} is the $1/f^3$ corner. The dual modulus prescaler needs to be able to operate at RF frequencies. The scaling of CMOS technology should take care of this problem [10]. Instead, the noise generated by the prescaler coupled to the nearby VCO is the major concern. A differential constant-current divider with reduced switching noise is preferred. The transfer function of a passive loop filter and the peak current that a charge pump can source/sink can be easily

adjusted to vary the loop bandwidth. A problem is that even though the output current of the charge pump is small, large capacitances may still be required to obtain a desired bandwidth. This makes integration of the loop filter difficult. Although use of an active filter can alleviate the requirement of large capacitances, the noise introduced by the operational amplifiers would couple back to the VCO and could hurt the phase noise performance.

To sum up, the basic requirements for a frequency synthesizer in the modern wireless communication system are high frequency accuracy, low-phase-noise, short acquisition time and low sideband spurs. Since the purity of a frequency synthesizer output is mainly determined by the VCO output spectrum, low-phase-noise CMOS VCOs consuming reasonable power must be first developed. Owing to the strong dependence of phase noise on Q's of the passive components present in the LC-tank of a VCO [9], research on high-Q passive components are essential. To further investigate and demonstrate the feasibility of integrated CMOS PLL frequency synthesizers operating at the multi-GHz frequency range and low supply voltages, a PLL including a low-phase-noise VCO, a low-switching-noise frequency divider, a PFD, a CP and a loop filter need to be constructed. The issues on implementation of high performance building blocks of a PLL frequency synthesizer and the interaction among these blocks should therefore be studied and understood. Implementation of a full CMOS frequency synthesizer with acceptable performance is one of the many steps toward the realization of a single chip radio.

1.2 Organization of this Dissertation

This work focuses on a CMOS RF frequency synthesizer. The primary goal is to integrate all components in a PLL based frequency synthesizer while achieving low voltage, low power and moderate phase noise for 5-GHz applications. The frequency targeted is ~5.5 GHz which is allocated by Federal Communications Commission (FCC) for wireless local area network (WLAN) and other industrial scientific and medical (ISM) applications. The specifications for applications at this frequency band have not been finalized. At such a high frequency, there are extreme challenges for implementing an integrated RF front end even using a BJT technology.

As mentioned in the previous section, the most challenging circuit block in a frequency synthesizer is the VCO. To better understand the contributions of phase noise in a VCO output spectrum, noise sources in a CMOS VCO must be identified. The relations between Q factors of passive components, power consumption and tuning range need to be understood. These fundamentals will be discussed in Chapter 2. One of the main difficulties for implementing an integrated synthesizer is the low quality factors of the passive components. For a capacitor, the Q is inversely proportional to the frequency, and capacitors may become the Q-limiting component rather than inductors at high frequencies. A design methodology and layout optimization techniques for overcoming the Q degradation are discussed in Chapter 3. Based on the results obtained in Chapter 2, guidelines for implementing a low-power and low phase noise VCO can be developed. VCOs operating at various frequencies

are presented in Chapter 4. The first two circuits are 900-MHz VCOs fabricated in a 0.8-μm CMOS technology. The phase noise is as low as -140 dBc/Hz at a 3 MHz offset, which is the lowest phase noise for a single stage VCO published to date. 5-GHz VCOs is also described. Their phase noise is once again the lowest reported to date for CMOS VCOs. A 25.9-GHz CMOS VCOs is also described in Chapter 4.

Finally, designs and experiments of the 5-GHz frequency synthesizer prototype including a VCO, an RF divider, a PFD, a charge pump and a loop filter will be completed using a 0.25-μm CMOS technology. A 5.5-GHz RF divider is designed such that the switching noise and power consumption are minimized. The charge pump should have small current glitches during switching between the UP and DN current sources while maintaining a sufficiently short transition time. A voltage doubler and level shift circuits are also designed and inserted into the PLL to increase the voltage range of the VCO control input, thus increasing the tuning range of the VCO/frequency synthesizer. Measurement results show that the divider and the voltage doubler have insignificant effects in the synthesizer output spectrum. The entire synthesizer works over the extended frequency tuning range from 5164.8 to 5536 MHz (371 MHz) due to the utilization of a voltage doubler. In addition, this work provided insights into the capabilities of CMOS technologies for RF applications at 5 GHz and beyond, and made contributions toward the implementation of a CMOS single-chip radio in the future.

CHAPTER 2
FUNDAMENTALS OF CMOS LC-OSCILLATORS

A voltage-controlled oscillator (VCO) is one of the most critical blocks in a frequency synthesizer. It mainly determines the phase noise performance of a frequency synthesizer outside the loop bandwidth. To design a VCO with good performance such as low phase noise, low power consumption, the fundamentals must be first understood. These include the basic principles of oscillation, relation between power consumption and device dimensions, effects from quality factor (Q) of the devices and identification of noise sources. In this chapter, these considerations will be discussed. Understanding of these fundamentals provides guidelines for designing high-performance VCOs. Phase noise measurement setups will also be briefly discussed.

2.1 Basic Principles of Oscillation

A basic oscillatory system is a closed-loop system with positive feedback. Figure 2-1 shows a structure of a sinusoidal oscillator consisting of an amplifier and a feedback network. Using a nodal analysis, the closed-loop transfer function can be shown to be

$$\frac{A(\omega)\beta(\omega)}{1 - A(\omega)\beta(\omega)} \tag{2.1}$$

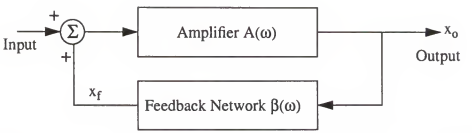


Figure 2-1 A basic oscillatory system consisting of an amplifier and a feedback network.

where $A(\omega)$ is the gain of the amplifier and $\beta(\omega)$ is the gain of the feedback network. Note that both $A(\omega)$ and $\beta(\omega)$ are frequency-dependent. By Barkhausen criterion [11], the denominator must be zero for oscillation to occur. Equating this, we have $1-A(\omega_0)\beta(\omega_0)=0$, known as the characteristic equation, where ω_0 is the resonant frequency of the network. It follows that $A(\omega_0)\beta(\omega_0)=1$ and $\angle A(\omega_0)\beta(\omega_0)= 2\pi \cdot n$ (or $\mathrm{Im}\{A(\omega_0)\beta(\omega_0)\}=0$) where n is an integer. The closed-loop transfer function has two poles at $j\omega_0$ and $-j\omega_0$, and the system oscillates at ω_0.

An intuitive explanation [11] for the oscillation is that for the system to sustain the output x_o (Figure 2-1) without an input signal, x_f ($=\beta(\omega_0)x_o$) must be sufficiently large so that $x_f A(\omega_0)$ equals to x_o. This again results in $A(\omega_0)\beta(\omega_0)=1$.

A conceptual implementation of the oscillator feedback loop is shown in Figure 2-2. The transconductor is assumed to be ideal, whose input impedance is infinite and output series impedance is zero. The corresponding open-loop voltage gain $A(\omega)=G_m Z_{RLC}(\omega)$ and feedback network gain $\beta(\omega)=1$ where G_m is

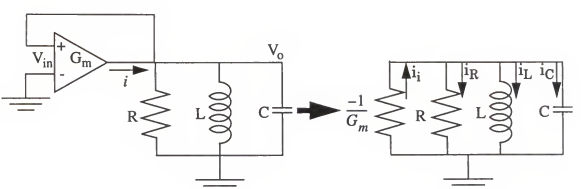


Figure 2-2 A conceptual implementation of the oscillator feedback loop

positive and real, and $Z_{RLC}(\omega)=\frac{j\omega LR}{R-\omega^2 LCR+j\omega L}$ is the total impedance of the RLC network. The characteristic equation becomes $G_m Z_{RLC}(\omega)=1$. The resonant frequency $\omega_0=\frac{1}{\sqrt{LC}}$ can be derived by solving $\mathrm{Im}\{A(\omega_0)\beta(\omega_0)\}=0$. The resulting $Z_{RLC}(\omega_0)=R$ and the characteristic equation is reduced to $G_m R=1$. The G_m satisfying this relation is the minimum transconductance required for oscillation to occur (critical oscillation), denoted as $G_{m,c}$. Another view point is that the amplifier generates current i (Figure 2-2) due to the input voltage V_{in} with a transconductance G_m (i.e. $G_m V_{in}=i$), the corresponding resistance looking into the output of the amplifier is $\frac{V_o}{-i}=\frac{V_{in}}{-i}=\frac{-1}{G_m}$ which is negative. The magnitude of the parallel negative resistance $\frac{-1}{G_m}$ is equal to R and cancels the loss in the RLC network. Hence, there would be no damping in the oscillatory system and the oscillation can be sustained.

For wireless communications, an RF VCO is typically required to have low noise performance. Thus, the number of devices which is also the number of noise sources is usually kept as low as possible. A differential structure is also desired to have better noise immunity. An example of a popular realization is shown in Figure 2-3(a). The transistors M1 and M2 are cross coupled to form a positive feedback network. Due to symmetry, the loop gain $A(\omega)\beta(\omega)$ is $(G_mZ_{net})^2$ (Figure 2-3(b)) where G_m is the effective transconductance of M1 and M2, and Z_{net} is the total impedance of the network consisting of an inductor, a varactor, and the parasitics associated with the transistors and passive components (not shown in Figure 2-3(a)). At resonant frequency, $(G_mZ_{net})^2$

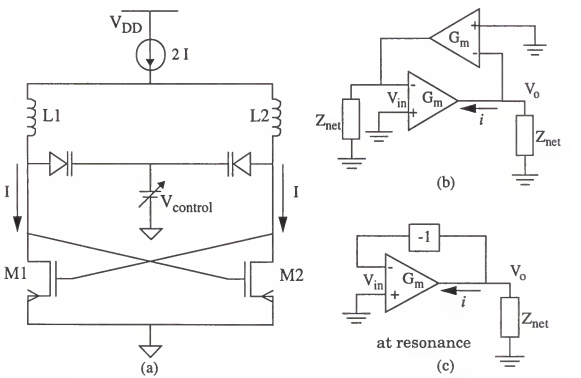


Figure 2-3 (a): An example of a popular realization of the differential negative-resistance LC-oscillator. (b): A simplified model of (a). (c): A simplified model of (b) at resonance.

must become unity. Thus, G_mZ_{net}=-1 (common source amplifier). Substituting the upper half of the circuit in Figure 2-3(b) by -1, the model in Figure 2-3(b) can be further simplified as shown in Figure 2-3(c). Using the simplified model, the loop gain $A(\omega)\beta(\omega)$ can be expressed as $-G_mZ_{net} \cdot (-1) = G_mR_{net} = 1$ where R_{net} is the real part of Z_{net}. This means that G_m must be equal to $G_{m,c}$ so that the product of G_m and the real loss in the network is unity. In a real CMOS oscillator, the voltage swing is typically large and the amplifiers are not ideal. The transistors actually act as loss components instead of amplifiers in some portion of a cycle. Effective G_m which may be different from the transconductance at the quiescent bias point as well as effective R, C, and loaded Q will be discussed in section 2.3.2.

2.2 Power Consumption of LC-Oscillators

2.2.1 Useful Transformations

The parasitic resistances of an inductor and a capacitor used in an LC-oscillator are generally in series with the reactive components. This may complicate the analyses and prevent designers from having intuitive ideas of the circuits. A transformation from series to parallel connections helps to alleviate this. The parallel forms of an inductor and a capacitor with their parasitic resistances will also be used for oscillator analyses in section 2.3.2.

Illustrated in Figure 2-4 are the desired transformations. The derivation is straight forward. By equating the total impedances of the networks, L_2

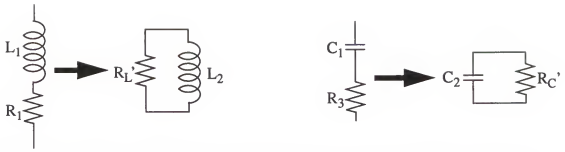


Figure 2-4 The transformation between series and parallel connections.

and R_L' can be expressed in terms of L_1 and R_1 as

$$L_2 = L_1 + \frac{R_1^2}{\omega^2 L_1} = L_1 \cdot \left(1 + \frac{1}{Q_L^2(\omega)}\right) \tag{2.2}$$

$$R_L' = \frac{\omega^2 L_1^2 + R_1^2}{R_1} = R_1 \cdot (1 + Q_L^2(\omega)), \tag{2.3}$$

where Q_L ($=\omega L_1/R_1=R_L'/\omega L_2$) is the quality factor of the inductor with its parasitic resistance. Similarly, C_2 and R_C' can be expressed in terms of C_1 and R_3

$$C_2 = \frac{C_1}{1 + \omega^2 R_3^2 C_1^2} = \frac{C_1}{1 + \frac{1}{Q_C^2(\omega)}} \tag{2.4}$$

$$R_C' = R_3 + \frac{1}{\omega^2 R_3 C_1^2} = R_3 \cdot (1 + Q_C^2(\omega)), \tag{2.5}$$

where Q_C ($=1/\omega C_1 R_3=\omega C_2 R_C'$) is the quality factor of the capacitor with its parasitic resistance. The LC network (Figure 2-5) used in a VCO typically consists of series parasitic resistances associated with the inductor and varactor. From Eqs. 2.3 and 2.5, the equivalent parallel parasitic resistances are proportional to Q^2 and the resonance frequency of the RLC network can be

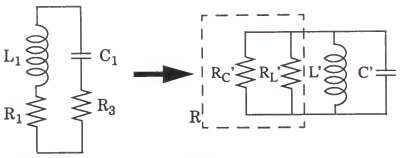


Figure 2-5 Transformation of a typical lossy LC-network to its equivalent RLC network.

obtained using Eqs. 2.2 and 2.4.

$$\omega_0 = \left. \frac{1}{\sqrt{L_1 \cdot \left(1 + \frac{1}{Q_L^{\,2}(\omega)}\right) \cdot \frac{Q_C^{\,2}(\omega) \cdot C_1}{Q_C^{\,2}(\omega) + 1}}} \right|_{\omega = \omega_0} = \sqrt{\frac{L_1 - C_1 R_1^2}{C_1 L_1^2 - R_3^2 C_1^2 L_1}} \qquad (2.6)$$

When R_1 and R_3 are zero, ω_0 is reduced to $1/\sqrt{L_1 C_1}$. The resistances of R_1 and R_3 typically have a minor effect on the resonant frequency ω_0.

2.2.2 Power Consumption versus C/L Ratio

Using the LC-oscillator model shown in Figure 2-2, relations between power consumption and capacitance/inductance ratio can be found. First, if one considers an LC network of a VCO with the parasitic series resistances associated with L_1 and C_1, the equivalent parallel RLC circuit model can be immediately derived using the transformations shown in the previous section (Figure 2-5). Typically, Q of the network in a monolithic VCO is dominated by that of the inductor. Thus, R (= $(R_C' \parallel R_L')$) may be approximated by R_L'. In

addition, two other approximations $L_1 = L'$ and $C_1 = C'$ can be made with less than ~8% errors between 1 and 20 GHz since Q_L^2 and Q_C^2 are typically larger than 12. To simplify the derivation, let $L_1/R_1=k$ where k is a constant for a given technology (this is true only for some types of inductors such as bondwires at low to moderate frequencies, and not strictly true for spiral inductors). Using Eq. 2.3, R at oscillation frequency ω_0 can be expressed as

$$R = Re(Z_{net}) = R_1 + \omega_0^2 k L_1 \tag{2.7}$$

Since $G_m Re(Z_{net})=1$ at ω_0 and R_1 is typically $<< \omega_0^2 k L_1$, the required G_m is inversely proportional to L_1. Hence, a larger L_1 or a smaller C_1/L_1 ratio for a given ω_0 requires smaller G_m and lower power consumption. Since $R_1=L_1/k$, Eq. 2.7 can be rewritten in terms of C_1

$$R = \frac{L_1}{k} + \frac{k}{C_1} = \frac{1}{C_1} \cdot \left(\frac{1}{\omega_0^2 k} + k \right) \tag{2.8}$$

It follows that the required G_m is proportional to C_1. A larger C_1/L_1 ratio for the same ω_0 needs more bias current to sustain the oscillation.

For a practical LC-oscillator, the total capacitance C consists of varactor capacitance αC where $0<\alpha<1$, and the parasitic capacitances $(C(1-\alpha))$ associated with the inductor and active devices, which are assumed to be constant. Assuming that the total inductance is L, C/L ratio is r, the equivalent parallel tank resistance is R and the tail current is 2I (Figure 2-3(a)), the tank amplitude V_{amp} is proportional to IR [12], [13]. If the varactor capacitance can be

tuned between $\chi\alpha C$ and αC where χ ($0<\chi<1$) is the capacitance ratio between minimum and maximum capacitances of a varactor for a given bias voltage range, the frequency tuning range can be expressed as

$$\frac{1}{\sqrt{L(C(1-\alpha)+\chi\alpha C)}}-\frac{1}{\sqrt{LC}}=\omega_0\left(\frac{1}{\sqrt{1-(1-\chi)\alpha}}-1\right) \qquad (2.9)$$

Now, if the total capacitance is changed to βC ($\beta>(1-\alpha)$) by increasing/decreasing the varactor capacitance while keeping the same ω_0 (the corresponding total inductance should be redesigned to be L/β), the equivalent tank resistance becomes R/β according to Eq. 2.8 if Q_C and R_C' are once again assumed to be much larger than Q_L and R_L'. The corresponding current to have the same tank amplitude is βI. The resulting frequency tuning range is

$$\frac{1}{\sqrt{\frac{L}{\beta}\cdot(C(1-\alpha)+\chi(\beta C-C(1-\alpha)))}}-\frac{1}{\sqrt{\frac{L}{\beta}\cdot\beta C}}$$
$$=\omega_0\left(\frac{1}{\sqrt{\chi+\frac{(1-\chi)(1-\alpha)}{\beta}}}-1\right) \qquad (2.10)$$

Hence, in order to increase the frequency tuning range, β must be increased so that the expression inside the square root decreases, resulting in larger power consumption. In addition, if the varactor capacitance is much larger than the total parasitic capacitance ($\alpha\rightarrow 1$), both Eq. 2.9 and 2.10 are equal to $\omega_0\left(\frac{1}{\sqrt{\chi}}-1\right)$. That is, the frequency tuning range for a given ω_0 is independent of the C/L ratio, and only depends on the varactor characteristics. The upper

limit of the frequency tuning range is $\omega_0\left(\frac{1}{\sqrt{\chi}}-1\right)$ when the total parasitic capacitance is negligible relative to the varactor capacitance. Therefore, decreasing C does not sacrifice the tuning range while decreasing the power consumption if the varactor capacitance is much larger than the total parasitic capacitance.

2.2.3 Noise Performance of an Oscillator

A figure of merit for the noise performance of an oscillator is phase noise which measures the short-term frequency stability of an oscillator. It is defined as $10 \cdot \log\frac{P_{sideband}(\omega_0+\Delta\omega)/Hz}{P_{carrier}}$ where $P_{carrier}$ is the carrier power and $P_{sideband}(\omega_0+\Delta\omega)/Hz$ is the total power in a 1-Hz bandwidth at an offset of $\Delta\omega$ from ω_0. The unit is dBc/Hz where dBc indicates a measurement in dB relative to the carrier power. Figure 2-6 illustrates the phase noise definition.

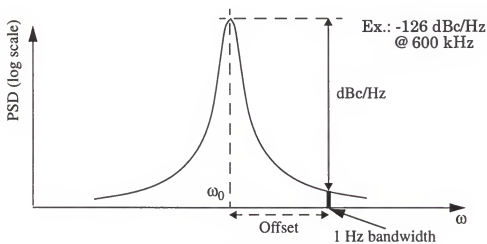


Figure 2-6 An illustration of definition of phase noise.

2.3 Q of LC Oscillators

2.3.1 Q of an Ideal LC Oscillator

From Barkhausen criterion, the oscillation frequency ω_0 is determined by the condition $\angle Z_{net} = 0$. Due to noise present in the oscillator, the criterion may not hold all the time. The characteristic of how the phase of the circuit changes with respect to the change of oscillation frequency ($\frac{d\phi}{d\omega}$) becomes one of the ways to measure the performance of an oscillator [11]. If $\frac{d\phi}{d\omega}$ is large, then a small change, $\Delta\omega$, results in a significant change of phase, $\Delta\phi$. This change in phase makes the VCO violate the Barkhausen criterion and in turn prevents the VCO from oscillating at $\omega_0+\Delta\omega$ Larger $\frac{d\phi}{d\omega}$ results in better concentration of energy at ω_0 and lower phase noise. This behavior represents the short-term frequency stability of an oscillator. Let the impedance of the LC-network shown in Figure 2-2 be H(ω). Differentiating $\phi = \angle H(\omega)$ with respect to ω and evaluating at ω_0, we have $\frac{S_F}{\omega_0} = \left.\frac{d\angle H(\omega)}{d\omega}\right|_{\omega = \omega_0} = \left.\frac{d\phi}{d\omega}\right|_{\omega = \omega_0}$ where S_F is the frequency stability factor. And the Q of the oscillator (also known as stability Q) can be defined as $\frac{S_F}{2}$ [14], [15], [16].

Since an LC-network is a band pass filter (BPF), another way to define the Q of an oscillator is to use the 3-dB bandwidth [15]. It is defined as the ratio of the center frequency to the two-sided-3-dB bandwidth, $\Delta\omega=\omega_1+\omega_2$,

where ω_0-ω_1 and ω_0+ω_2 are the frequencies at which the magnitudes of $H(\omega)$ are $\frac{1}{\sqrt{2}}$ of that at ω_0. If Q is high, there will be large attenuation on the skirt of the oscillator output spectrum resulting in lower phase noise.

2.3.2 Q of a Nonideal LC Oscillator

The above two Q definitions can be easily applied to any ideal oscillator whose active device(s) has (have) infinite output resistance and the capacitances and resistances present in the LC tank have no voltage dependence. However, a real oscillator fabricated using semiconductor devices typically has finite output resistance from the active device(s). The parasitic capacitances associated with the active device(s) and the varactor capacitances typically have strong voltage dependence as well. The non-ideality of the elements introduces nonlinearity to the LC tank making it difficult to estimate the loaded Q using the definitions mentioned previously. Moreover, due to a large signal swing, the active devices in an oscillator, for example Figure 2-3(a), act as an energy provider for approximately a half period (T/2 where T is the inverse of the oscillation frequency f_0) while act as a resistor or open for the other T/2 as illustrated in Figure 2-7. That is, the output resistances of the transistors are also voltage dependent. Hence, the loaded Q, effective G_m and effective tank resistance and capacitance could be significantly different from those at quiescent bias condition.

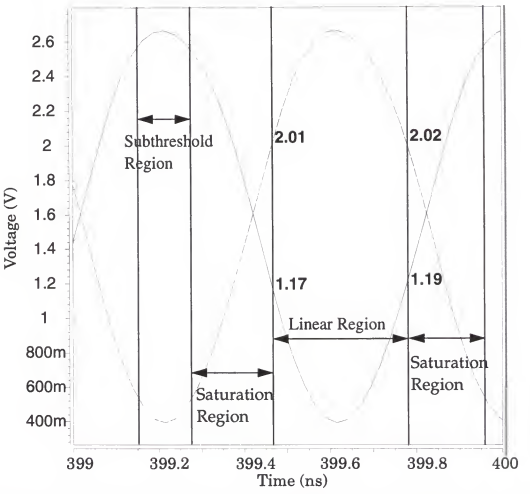


Figure 2-7 An illustration of the bias conditions of active devices in an oscillator.

2.4 Noise Sources in CMOS Oscillators

2.4.1 Flicker (1/f) Noise

In MOS transistors, the mobility and carrier number fluctuations result in high flicker (1/f) noise [17], which poses problems for attaining low close-in phase noise in CMOS VCO's. Figure 2-8 shows the normalized (to 1-μm width) input-referred 1/f noise spectra for NMOS and buried channel PMOS transistors from the 0.8-μm CMOS process at $|V_{GS}|$ and $|V_{DS}|$ of 1.0 and 2.0 V (in

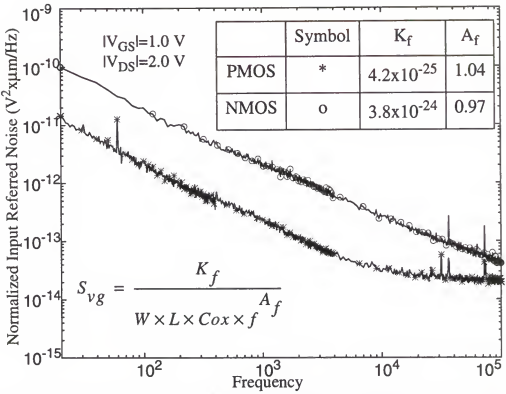


Figure 2-8 Noise spectra of a PMOS and a NMOS transistor at $|V_{GS}|$=1.0 V and $|V_{DS}|$=2.0 V.

saturation region of operation), respectively [18]. The input-referred 1/f noise S_{vg} is calculated by dividing measured output (current) noise S_{Id} by g_m^2. The PMOS flicker noise is around one order of magnitude lower than the noise of the NMOS transistor with a surface channel. If the dc bias current were kept the same for the transistors by adjusting the widths, the difference would have been even greater. Using the simple theory [19]

$$S_{vg} = \frac{K_f}{W \times L \times Cox \times f^{A_f}}, \qquad (2.11)$$

the extracted K_f parameters for the NMOS and PMOS transistors are $3.8x10^{-24}$ and $4.2x10^{-25}$ V^2F, respectively.

For a deep submicron CMOS process, both NMOS and PMOS transistors are surface channel devices, and a concern is that PMOS may have the same poor 1/f noise performance as NMOS transistors. However, measurements show that the PMOS 1/f noise is ~8-10 times smaller at 100 kHz for the same transistor dimension and gate over drive (V_{GT}=V_{GS}-V_T) when the V_{GT} is smaller than ~0.3 V [18]. In addition, when comparing NMOS and PMOS transistors for oscillator applications, the LC-tank, G_m and I_D should be kept the same. The required channel width of a PMOS transistor is larger than that of an NMOS transistor due to the mobility difference. Hence, PMOS transistors still have the advantage of attaining low close-in phase noise in oscillator applications. As the devices are scaled down below ~0.5 μm, Eq. 2.11 does not hold. The dependence of L and C_{ox} becomes stronger, and thus, 1/f noise is higher for shorter channel devices [17], [18], which is an additional concern for VCO built using these technologies.

2.4.2 Channel Thermal Noise

Thermal noise in a MOS transistor originates from the resistive channel. It is white and may be expressed as $\overline{i^2} = \gamma 4kTg_m\Delta f$ where γ is a constant, k is the Boltzmann's constant and T is the temperature. The constant γ is 2/3 for long channel devices and is typically significantly greater than 2/3 (increases as $\frac{1}{L^a_{eff}}$ where L_{eff} is the effective channel length and a may be between 2 and 3) for short channel devices due to the hot electron effect [17].

Unlike the phase noise in $1/f^3$ region (contributed from 1/f noise) which may be reduced by a PLL (Figure 1-5), the phase noise converted from the thermal noise in $1/f^2$ region is typically outside the loop bandwidth and will not be suppressed by the PLL. According to [20], the hot electron effect for a PMOS transistor is smaller than that of an NMOS transistor because the impact ionization rate of electrons is 1-2 orders of magnitude higher than that of holes. Thus, PMOS is once again should be the preferred device for oscillators.

2.4.3 Noise from Power Lines and Substrate Coupling

When noise exists in the power and ground connections, the phase noise of an oscillator tends to be degraded even if the oscillator has a differential structure. There are two sources responsible for this [21]. One is the voltage-dependent drain-to-body capacitance, C_{db}, which senses the noise in power and ground lines, and translates it to FM noise and thus phase noise. The other is the insufficient common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) of the amplifier. The noise in the substrate is coupled in the same way as the supply noise. To reduce the noise coupled from supply and substrate, large bypass capacitors for dc lines and lots of substrate contacts surrounding the oscillator are needed to provide low-impedance grounding paths. The sensitivity of the oscillatory frequency to the supply voltage is called frequency pushing, and is expressed in Hz/volt.

2.4.4 Noise/Effects from the Load

If an oscillator is not buffered, the noise in the load or subsequent circuit block which may be much larger than that of a buffer for the VCO can contributes significant noise back to the oscillator core. Another more serious problem is the injection locking. This happens when there is a strong signal at ω_s injected into the output port of the oscillator. The oscillator signal will tend to change frequency and will eventually lock onto ω_s if ω_s is within the pull-in range of the oscillator [22]. The last effect from the load is the frequency pulling which is due to a non-ideal load. That is, the oscillation frequency can be changed if the load changes its impedance from time to time or periodically. Hence, adding a buffer can improve the isolation although the buffer also adds noise.

2.4.5 Noise from the Bias Circuit

The bias current of an oscillator is typically controlled by a current source as shown in Figure 2-3(a). The noise from this current source can vary the G_m of the cross-coupled transistors and cause AM noise which may be converted into phase noise [23], [24]. Since the noise is common mode in nature, it may also vary the voltage across the tuning device resulting in FM noise and thus phase noise. In addition, the reference current generator and current mirror typically consist of many devices. Its output noise can directly modulate the output of the current source, and can further increase the phase noise.

It has been shown that the noise due to a bias circuit can contribute as high as 15% to the oscillator phase noise [24].

2.5 Phase Noise Measurement

Phase noise can be measured in different ways. Batteries are typically used as power supply of the device under test (DUT). The simplest method is to measure using a spectrum analyzer. However, there are limitations associated with the dynamic range and the fact that the input signal from a free running VCO may not be stable. The details as well as measurement using more sophisticated systems are described in this section.

2.5.1 Spectrum Analyzer

The simplest way to measure phase noise of an oscillator is to directly connect the DUT to a spectrum analyzer. This measures the short-term frequency stability of an oscillator. A spectrum analyzer measures the total power (P) in a frequency band referred to as the resolution bandwidth (RBW) which can be changed by users. The unit of the spectral density displayed on a spectrum analyzer is thus typically dBm/(RBW Hz). To compute the phase noise, the relative power level, P_r, at an offset frequency from the carrier is measured relative to the carrier power. It is then normalized to dBc/Hz by subtracting $10\text{x}\log_{10}(\text{RBW})$ from P_r. An assumption is that the power spectral density over the RBW is flat (white). The first limitation with this method is that the noise floor of the measurement system is limited by the LO of the

spectrum analyzer. With a synthesized LO, a modern spectrum analyzer such as HP8563E has a sensitivity of ~-149 dBm at 1 GHz. The second limitation is the measurable phase noise which is limited by the dynamic range of the spectrum analyzer. The dynamic range comes from the maximum allowed input power to the mixer (p_{max}) in a spectrum analyzer and the sensitivity of a spectrum analyzer. This limitation can be improved by the methods described in the following sections.

2.5.2 Phase-Locked Loop

To improve the dynamic range limit discussed above, a phase noise measurement setup with an external low noise source and a comparator can be used. A simplified configuration is shown in Figure 2-9. The basic principle of this method is to down convert the DUT output to baseband using a PLL formed by a low noise reference source, a phase detector and a narrow band

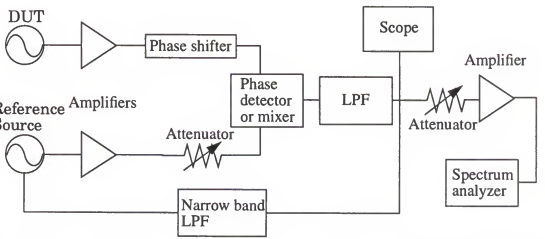


Figure 2-9 A simplified configuration of phase noise measurement setup with an external low-noise reference source and a comparator.

low pass filter so that the strong carrier power is rejected, thus eliminates the dynamic range limitation due to a large carrier power. The measurable phase noise will then be limited by the sensitivity of the spectrum analyzer. The bandwidth of the narrow band filter (which is programmable in some measurement systems) must be narrow enough (typically less than 100 Hz) so that the measured sideband represents the true oscillator sideband instead of the PLL sideband. The phase noise of the reference source obviously needs to be much lower than that of DUT. The amplifiers are necessary to avoid injection locking between the two sources. This configuration still suffers the limitation of system noise floor which is due to phase noise of the reference source and LO of the spectrum analyzer.

2.5.3 Frequency Discriminator

A phase noise measurement setup using a discriminator could give a better noise floor because there is no reference source needed in the system. Similar to the set-up using an external low noise reference source, the dynamic range limit can be improved. Figure 2-10 shows the setup. This method is also referred to as the autocorrelation method since the signal at the output of the double balanced mixer has the form of $E[x(t)x(t+\tau_d)]$ [25] which represents the power spectral density of the random process after being converted to frequency domain. A disadvantage is that the noise floor tends to be degraded for low offset frequencies [26].

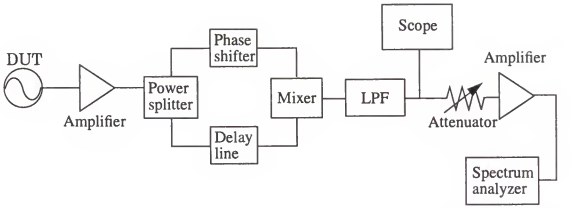


Figure 2-10 A phase noise measurement setup using a frequency discriminator.

2.6 Summary

In this chapter, basic principles of LC-oscillators were discussed. The relationship between power consumption and C/L ratio of an LC-tank which also directly influences the tuning range of a VCO was derived. This gives a guideline for choosing inductance and capacitance values when designing a VCO. A major factor in an oscillator design is the quality factor of the LC-tank. The effect of Q on oscillator power consumption was discussed. To better understand the contributions of phase noise in an oscillator, the noise sources in CMOS oscillators were identified. Finally, phase noise measurement setups were briefly presented. These discussions provide basic guidelines to improve the design and measurements of VCOs.

CHAPTER 3
PASSIVE COMPONENTS

3.1 Introduction

As discussed in CHAPTER 2, radio frequency (RF)/microwave integrated circuits, passive components are crucial to the circuit performance. Quality factor (Q) of the passive components strongly affects the characteristics of the circuit such as phase noise of voltage controlled oscillators (VCOs) and tuned response and power gain of low noise amplifiers (LNAs). However, due to significant parasitics, frequency-dependent capacitor reactance, and losses in p^+ silicon substrates, it is difficult to achieve high quality factor at GHz frequency range in CMOS technology. Passive components should be linear for a wide voltage range so that the circuits using the components can have a wide dynamic range. Additionally, the passive components should be inexpensive, area-efficient, and easy to implement and to utilize in order to reduce the total cost in the design and fabrication phases. For some applications such as for bypassing of the power and ground line inductances, quality factors of the capacitors should be limited to avoid/damp unwanted resonance [27]. Hence, the flexibility of controlling quality factors using a given structure is also desired in order to reduce the design complexity. In this chapter, design, implementation, and layout optimization of high-Q capacitors, high-Q

varactors, as well as improvements of quality factors of transistor parasitics in CMOS technologies are discussed. The expressions for quality factors of the passive components are presented. A pad structure with a ground shield is presented in section 3.2.4. The ground shield underneath a pad essentially eliminates the unwanted electrical coupling between the pad and substrate. Hence, for test structures, it reduces measurement and extraction errors of model parameters. It also reduces unwanted signal coupling through substrate and improves the circuit performance [28]. Finally, considerations for designing on-chip spiral inductors are summarized in section 3.5.

3.2 High-Q MOS Capacitors

As mentioned above, a required passive component for RF applications is an inexpensive, area-efficient and high-Q (quality factor) capacitor which is easy to implement and utilize. The capacitors should also be linear and have low parasitic capacitance. To address this need, metal-to-metal capacitors with a Q-factor of 80 at 2.5 GHz in a BiCMOS process [29] and polysilicon-to-n^+-plug capacitors in a bipolar process [30] have been discussed. The former structure suffers from a low capacitance/area and a relatively large parasitic capacitance while the latter structure is not available in conventional foundry CMOS processes and requires additional processing steps. In this section, using a conventional foundry 0.8-μm CMOS process, capacitors with a Q greater than 100 at 900 MHz and with a high intrinsic capacitance/area (~200 nF/cm^2) is discussed [31]. This was accomplished by optimiz-

ing layouts of a naturally available polysilicon-to-n-well MOS capacitor structure which has been commonly dismissed for RF applications due to the high n-well sheet resistance. To further demonstrate their usefulness for RF and microwave applications, the capacitor structure was utilized in a 3-V 900-MHz LNA similar to the LNA in [32] with excellent results. The capacitor was also used in VCOs for frequency tuning and will be discussed in CHAPTER 4.

3.2.1 Approach

Figure 3-1 shows a top view, a cross section and an equivalent circuit model of an MOS capacitor test structure. Top and bottom plates of the capacitor are formed with silicided polysilicon and n-well, and are separated by a gate oxide (SiO_2) layer. C_{pad} and R_{psub} represent parasitic capacitance and resistance associated with probe pads of the test structure. Since the gate oxide layer is very thin (thickness of ~17 nm), the capacitor has a high intrinsic capacitance/area especially if it is biased in the accumulation region [33]. Because of this, the structure can also have a high ratio between capacitance and parasitic capacitance associated with the n-well-to-substrate junction. If the capacitor is not biased in the accumulation, the capacitance will decrease by a factor of around two due to formation of a depletion region under the gate oxide [33]. The series resistance (R_s) originates from resistances of the silicided polysilicon gate ($R_{poly,\square}$, ~2.3 Ω/□), n-well ($R_{nw,\square}$, ~1.1 kΩ/□), vias, contacts (R_{cont}) and metal lines. Excluding the via, metal and contact resistances,

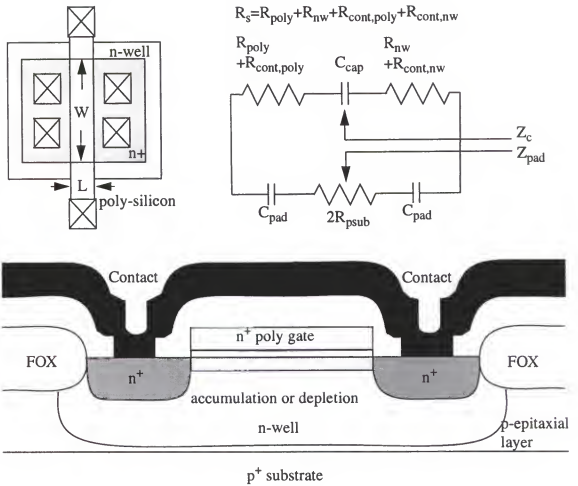


Figure 3-1 A top view, a cross section and an equivalent circuit of the MOS capacitor structure.

and gate-bias dependence of the n-well resistance [33], the series resistance of the capacitors can be approximated as

$$R_s = \frac{1}{3}\times\frac{1}{2}\times\frac{1}{2}\times\frac{1}{N}\times\left(R_{nw,\square}\times\frac{L}{W}+R_{poly,\square}\times\frac{W}{L}\right) \tag{3.1}$$

where N is the number of capacitor stripes, L and W are the length and width of the stripes (Figure 3-1), and $R_{nw,\square}$ and $R_{poly,\square}$ are the sheet resistances of the n-well and silicided polysilicon gate layers, respectively. The 1/3 factor

accounts for the spreading effect (APPENDIX A) while two 1/2 factors account for double-sided contacts for the n-well and gate layers. For a required capacitance and thus an MOS capacitor area (A), N is equal to A/(LxW). Substituting this into Eq. 3.1, R_s can be expressed as a function of L and W

$$R_s = \frac{1}{12 \times A} \times (R_{nw,\square} \times L^2 + R_{poly,\square} \times W^2) \tag{3.2}$$

As will be presented later, the overlap ($C_{overlap}$) and fringing ($C_{fringing}$) capacitances need to be taken into account to calculate the required gate area A in a deep submicron CMOS process since the contributions of $C_{overlap}$ and $C_{fringing}$ are larger resulting in a smaller gate area A and higher resistance R_s.

Since $R_{nw,\square}$ is much larger compared to $R_{poly,\square}$, the $R_{nw,\square}xL^2$ term typically dominates the total series resistance. When W/L ratio is large, $R_{nw,\square}xL^2$ could become comparable to $R_{poly,\square}xW^2$. To minimize R_s, both L and W need to be as small as possible. Using Eq. 3.2, quality factors of the capacitors (Q) can be expressed as

$$Q = \frac{1}{\omega C R_s} = \frac{12}{\omega \times c_{unit} \times (R_{nw,\square} \times L^2 + R_{poly,\square} \times W^2)} \tag{3.3}$$

where ω is the frequency and c_{unit} is the intrinsic capacitance/area. When the minimum dimensions of L and W are used, Q is the maximum. However, penalties are larger overall required area and n-well-to-substrate parasitic capacitance because of an increased number of contacts. As stated, the contact resistances are not included in the analysis since they are typically small

($=R_{contact}/N_c$ where $R_{contact}$ is the resistance of a single contact and N_c is the number of contacts). If needed, they can easily be included.

In order to experimentally examine these, capacitor test structures were designed and fabricated. Capacitor values of ~140 fF which are relatively small have been chosen to reduce impact of contact resistances between pads and microwave measurement probes. The small capacitor values, however, introduced inconsistencies in capacitor measurements below around 2.5 GHz. Capacitor areas (excluding contact areas) were 3x1.2x13.6 (48.9) μm^2 (High-Q), 2.4x24 (57.6) μm^2 (Medium-Q) and 9.2x5.6 (51.5) μm^2 (Low-Q). Figure 3-2(a) shows the layouts of the three capacitors on the chip, while Figure 3-2(b) shows a detailed layout of the High-Q capacitor.

3.2.2 Results and Discussion

One-port S-parameter data of the capacitors and open structures (pad frame) were collected using an HP8510C network analyzer. The open structures are the same as the capacitor structures except that there are no interconnects between capacitors and pads. Due to substrate coupling, the circuit model in Figure 3-1 does not exactly match the capacitors under test in the measurement system, and the impact will be discussed in the next section. The S-parameter data were converted to admittances. To de-embed effects of the pad frame, admittances of the open structures are subtracted from the measured total admittances since the pad parasitics are connected in parallel

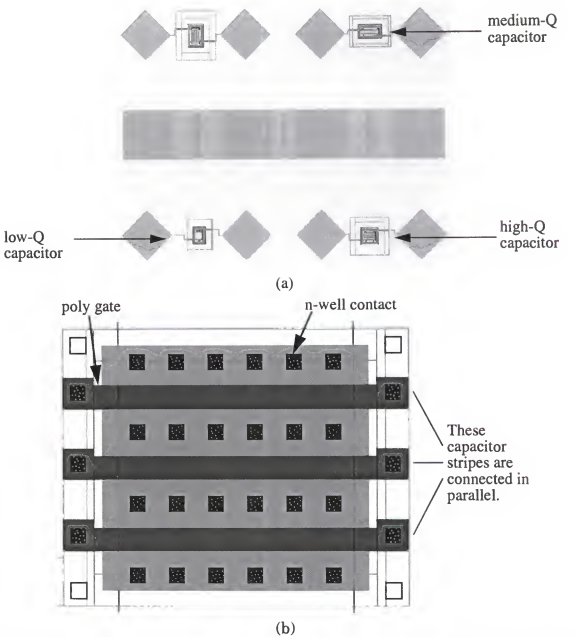


Figure 3-2 (a): A capacitor microphotograph. (b): A high-Q capacitor layout. The area excluding contacts is 3x1.2x13.5 μm^2.

according to the model shown in Figure 3-1. This method does not de-embed the probe contact resistance, thereby over-estimating the series resistances and under-estimating the quality factors. Using the corrected admittance data (y_{11}), resistances and capacitances were then extracted from the real and

imaginary parts, respectively. The measured MOS capacitances versus frequencies between 3 and 4 GHz are shown in Figure 3-3(a) while the same for the parasitic n-well-to-substrate junction capacitances are shown in Figure 3-3(b). The extracted capacitance values were essentially constant over the frequencies between 3 and 4 GHz. Figure 3-4(a) shows capacitances averaged over a frequency range between 3 and 4 GHz versus bias plots. The plots show the expected high frequency C-V characteristics. For dc voltages greater than 1 V and lower than -0.5 V, the capacitors are quite linear. With proper biases, the capacitors can have a good linearity and a high intrinsic capacitance/area value. The capacitances are higher than the simulated by ~9% due to an incorrect open structure (section 3.2.3). Standard deviations of the averaged capacitances in percent are shown in Figure 3-4(b). The standard deviation was computed using the measured data between 3 and 4 GHz to evaluate the fluctuation thus quality of the data over the measured frequency range. The highest standard deviation of 2.7% indicates that the quality of measurements is good. Figure 3-5(a) shows the series resistances of MOS capacitors measured at frequencies between 3 and 4 GHz and a 3-V bias. The resistances, like the capacitances, are essentially constant over the frequency range. Figure 3-5(b) shows the resistance versus frequency plots for the parasitic capacitors. The extracted resistances decrease ~10% between 3 and 4 GHz due to an incorrect open structure (section 3.2.3). Averaged series resistances for the MOS capacitors (over the same frequency range as the capacitances) are plotted versus bias between the top and bottom plates in Figure 3-6(a). Increasing the gate

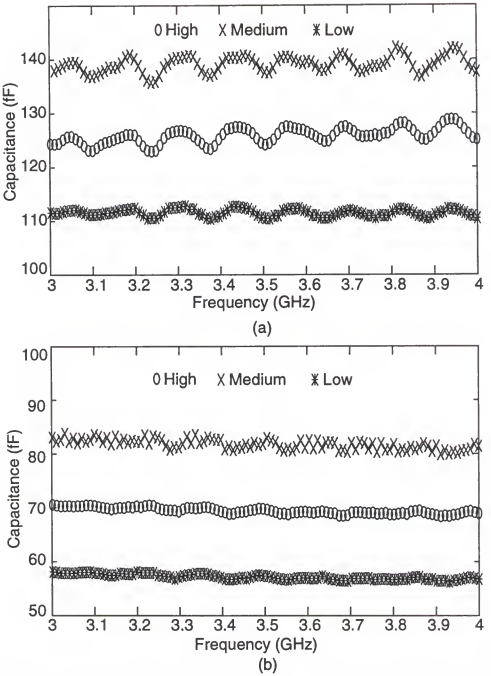


Figure 3-3 (a): Capacitance versus frequency plots of the high, medium and low-Q capacitors. The variations are small over the 3 to 4 GHz frequency range. (b): Parasitic capacitance versus frequency plots of the high, medium and low-Q capacitors. The variations are small over the frequency range between 3 and 4 GHz.

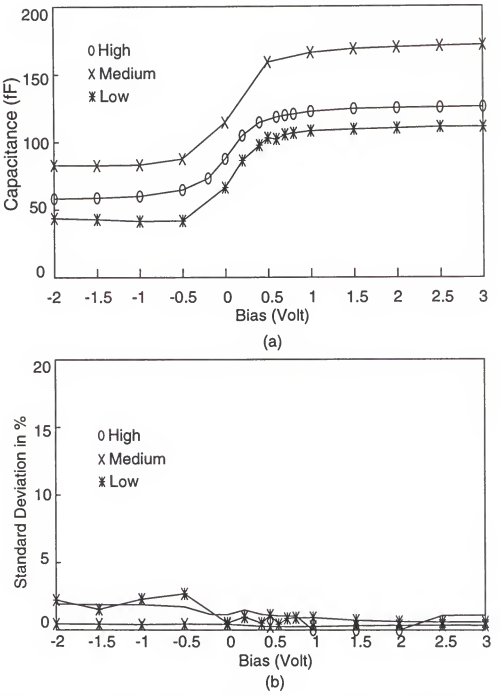


Figure 3-4 (a): A high-frequency MOS C-V characteristics. When dc voltages are greater than 1 V, the capacitors are quite linear. (b): Standard deviation of the averaged capacitances versus bias plots for the high, medium and low-Q capacitors. These low values indicate that the measurements are reliable.

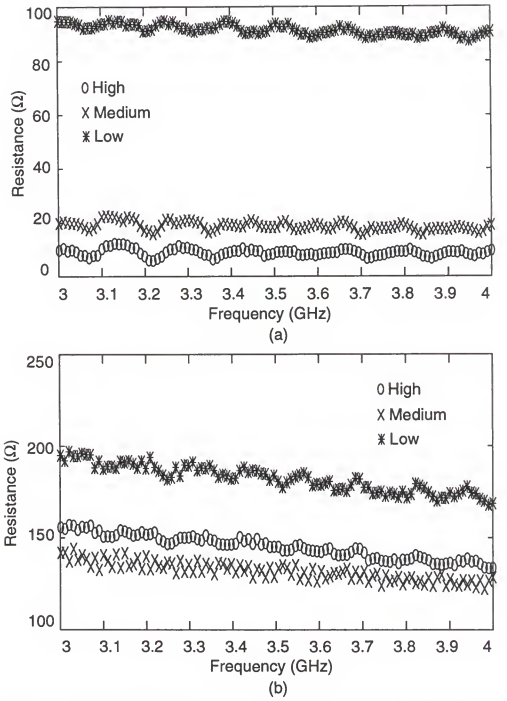


Figure 3-5 (a): Measured resistance versus frequency plots of the high, medium and low-Q capacitors. The variations are small over the 3 to 4 GHz frequency range. (b): Parasitic resistance versus frequency plots of the high, medium and low-Q capacitors. The variations are small over the frequency range between 3 and 4 GHz.

(top plate) bias voltage decreases the depletion layer width and increases the electron concentrations of the n-well under the gate region (accumulation), thus decreasing the n-well resistance. The resistances decreased by 30% to 40% depending on structures as the top plate voltage was increased from 0.4 to 3 V. Standard deviations in percent are shown in Figure 3-6(b). The standard deviations are computed using the measured data similar to that for the gate capacitances and are less than 3% except for the high and low bias ranges of the high-Q capacitor implying that the measurements are reliable.

Quality factors at 3 GHz were extracted using $Im(y_{11})/Re(y_{11})$ definition and were 49, 14 and 5 for High, Medium and Low-Q capacitors respectively. Normalized quality factors (1/RC or ωQ) are also extracted by multiplying ω and $Im(y_{11})/Re(y_{11})$. The normalized Q-factors as a function of bias are obtained once again by averaging over frequencies between 3 and 4 GHz for each bias. The Q values at 900 MHz were then extrapolated by dividing the normalized Q by $\omega=2\pi$ x 900 MHz. Figure 3-7(a) shows the normalized Q and extrapolated Q-factors at 900 MHz versus bias. At a 3-V top-plate bias, the extrapolated Q values for the high, medium and low-Q capacitors are 160, 46 and 17. If the contact and interconnect resistances between the capacitors and microwave probes were subtracted, the Q values would have been even higher. Standard deviations are shown in Figure 3-7(b). Because the series resistance of the High-Q capacitor is small, the data were noisier compared to those of the Medium and Low-Q capacitors. Since the High-Q capacitor needs more contacts, the ratio between the capacitance and total capacitor area was lower.

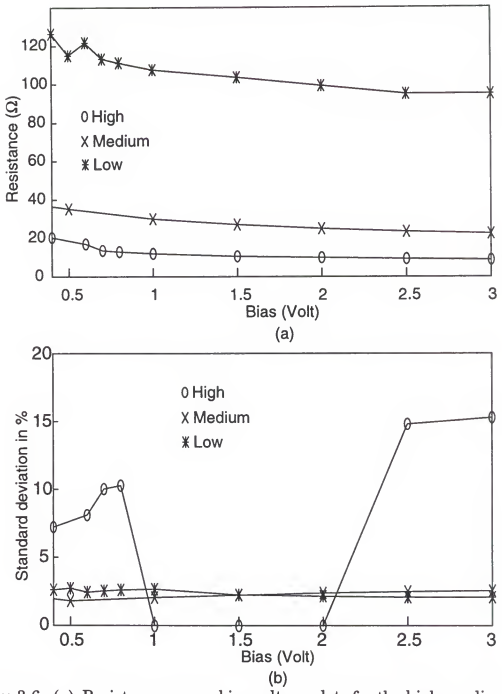


Figure 3-6 (a): Resistance versus bias voltage plots for the high, medium and low-Q capacitors. The electron concentration under the gate region increases with the bias voltage, thus reducing the resistance. (b): Standard deviation of the averaged resistances versus bias plots for the high, medium and low-Q capacitors. The standard deviations are less than 3% except for the high and low bias ranges of the high Q capacitor, which indicates that the measurements are quite reasonable.

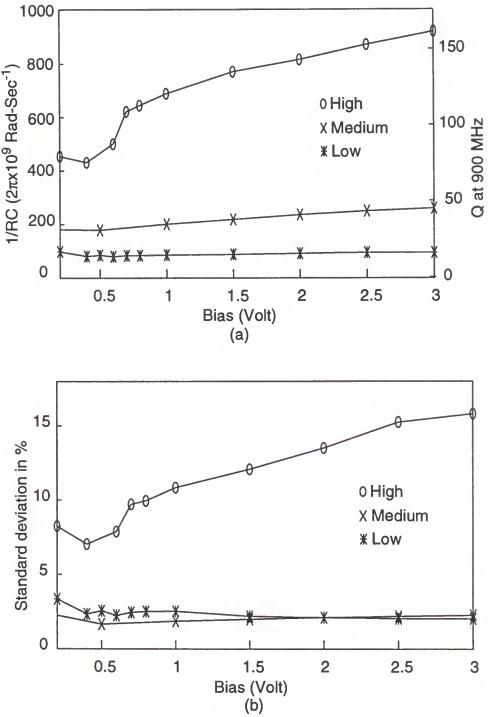


Figure 3-7 (a): Normalized quality factors (ωQ) and standard deviations versus bias plots of the high, medium and low-Q capacitors. The ωQ was extracted by multiplying ω with $\mathrm{Im}(y_{11})/\mathrm{Re}(y_{11})$. The Q values at 900 MHz were extrapolated using this ωQ. All the data were averaged over frequencies between 3 and 4 GHz. (b): Standard deviations of the averaged ωQ.

The ratios for the High, Medium, and Low-Q capacitors were 53, 73, and 88 nF/cm^2. These were low-end values since the design values of the capacitors were small and number of n^+ diffusion stripes was ~1.3 times of polysilicon stripes. For larger high-Q capacitors, the ratio between number of n^+ diffusion and polysilicon stripes should approach 1. The corresponding capacitance/area ratio becomes ~70 nF/cm^2, which are substantially higher than the metal-to-metal capacitors [29] and comparable to that of the polysilicon-to-n^+-plug capacitors [30].

Figure 3-8(a) shows averaged capacitances versus bias plots for the n-well-to-substrate parasitic capacitors. As expected, the capacitances decrease with the bias voltage due to an increase in the depletion layer width. They were relatively large due to un-optimized n-well layouts and small design values for the capacitors resulting in parasitic capacitances being dominated by the perimeter components. When optimized, the ratios for the high, medium and low-Q capacitors at a reverse junction voltage of 0.0 V should become around 2.4, 3, and 3 respectively. Of course, at a higher reverse junction voltage, the ratios will be higher. Figure 3-8(b) shows standard deviation plots. The maximum standard deviation is ~1% which demonstrates consistency of the data (small measurement fluctuation).

Table 2-1 summarizes the measured resistances, capacitances and Q-factors $Im(y_{11})/Re(y_{11})$ at 3 GHz, and extrapolated Q-factors at 1 GHz for the MOS capacitors. The Q-factors at 1 GHz were extrapolated by multiplying the 3 GHz data by a factor of 3. The Q factors at 1 GHz were calculated for the

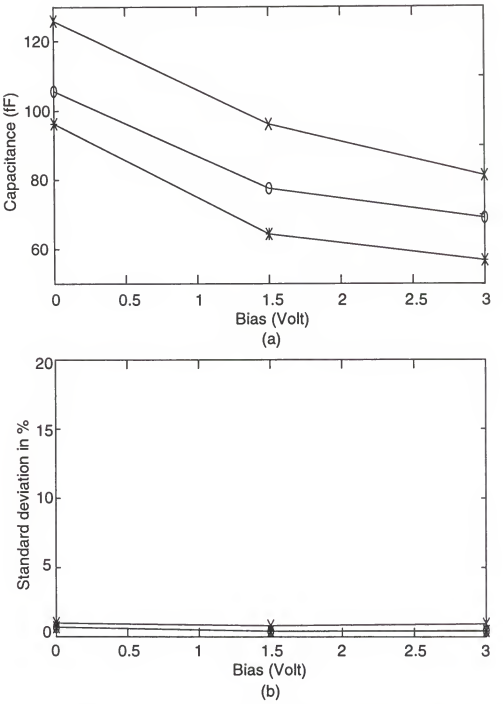


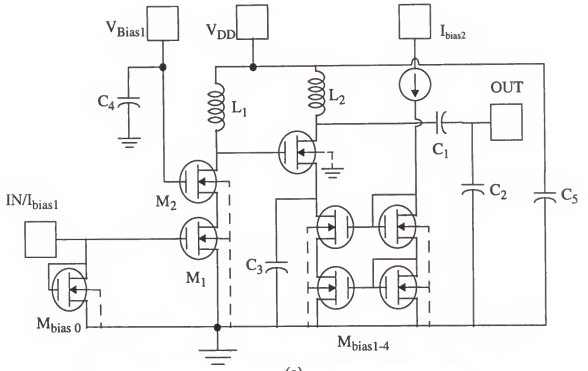
Figure 3-8 (a): Measured parasitic capacitances and standard deviations versus bias plots of the high, medium and low-Q capacitors. The capacitance decreases with the n-well-to-substrate reverse junction voltage. (b): Standard deviations of the averaged parasitic capacitances. The ~1% maximum deviation implies that the measurements are reliable.

design of LNA below. The measured parasitic capacitances associated with the n-well-to-substrate junction at zero and 3 V biases are also listed in Table 2-1. The table also lists estimated parasitic capacitances when the n-well layouts are optimized. The parasitic capacitances of the optimized structures are around a half of the measured values. Furthermore, if the design values for capacitors are increased by 10X, the ratio of MOS to parasitic capacitance should increase by another factor of 2~3 due to the fact that as capacitor values are increased, the parasitic capacitance becomes dominated by the area rather than perimeter component.

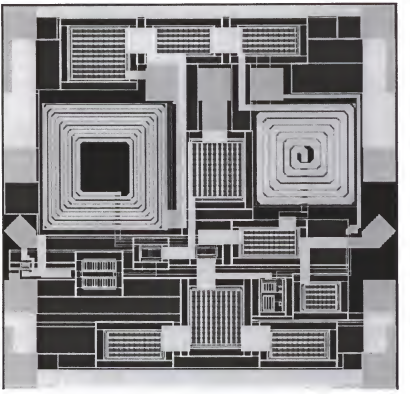
Table 2-1: A summary for MOS and parasitic capacitors.

	MOS CAP.		PARASITIC CAP.			
	Measured at 0.5V	Measured at 3V	Measured Data (Ω, fF)		Opt. Cap. (fF)	
			0 V	3 V	0 V	3 V
High	R=19Ω C=116fF Q=24.22 @ 3GHz Q=72.66 @ 1GHz	R=9Ω C=126fF Q=47.2 @ 3GHz Q=141.6 @ 1GHz	R=179 C=106	R=140 C=69	53	37
Med	R=35Ω C=159fF Q=9.455 @ 3GHz Q=28.37 @ 1GHz	R=23Ω C=172fF Q=13.75 @ 3GHz Q=41.26 @ 1GHz	R=154 C=126	R=128 C=81	58	40
Low	R=116Ω C=103fF Q=4.43 @ 3GHz Q=13.29 @ 1GHz	R=92Ω C=112fF Q=5.14 @ 3GHz Q=15.42 @ 1GHz	R=197 C=96	R=176 C=57	38	27

Figure 3-9 shows a schematic and a layout of a 3-V LNA utilizing the capacitors [31], [34]. The circuit consists of two amplifier stages, a capacitive transformer at the output, and bias circuits. The transducer power gain and noise figure at the resonant frequency of 960 MHz were 16.2 dB and 3.5 dB,



(a)



(b)

Figure 3-9 (a): A low noise amplifier (LNA) schematic. (b): An LNA layout.

respectively. The second stage biasing circuit is bypassed using a 40-pF MOS capacitor (C_3) to improve the stability. The top plate voltage is ~1.4 V and the capacitor is in the accumulation region resulting in a high capacitance/area value. An output capacitor transformer is used for dc isolation and to improve the output matching with a negligible gain degradation. The values of C_1 and C_2 were 10.7 and 7.5 pF, respectively and they were formed using MOS capacitors and associated parasitic capacitors. Top and bottom-plate dc biases of C_1 were ~2.7 and 0 V, respectively while those of C_2 were 0 V. The 0-V dc bias on the bottom plate of C_1 is consistent with typical applications of the LNA in which it drives a passive filter. To investigate the linearity dependence of the gate bias of M_2, a pad for V_{Bias1} is provided. A 20-pF capacitor (C_4) is included to bypass parasitic inductances and to ac-ground the gate of M_2. Lastly, a 20-pF capacitor (C_5) is used to bypass parasitic inductances associated with the supply and ground. Connecting the top plate to the supply and the bottom to ground ensures that the capacitor is biased in the accumulation. Figure 3-9(b) clearly shows that a majority of the circuit area is occupied by inductors and capacitors, high-lighting a need for area-efficient capacitors and inductors.

A concern for the MOS capacitor structure and associated parasitic n-well-to-substrate junction capacitance is the linearity which can reduce the 1-dB compression (P_{1dB}) (Figure 3-10) and third-order intermodulation intercept (P_{IP3}) points of amplifiers. The measured P_{1dB} compression point of the

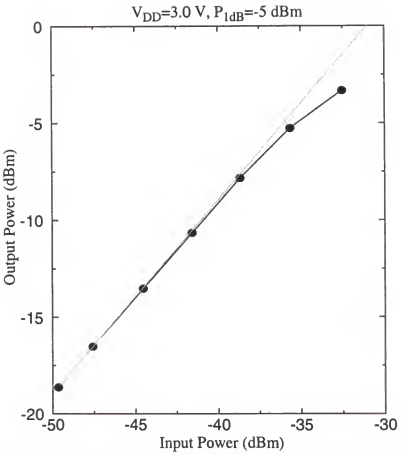


Figure 3-10 An output power versus input power curve for the LNA. The P_{1dB} and P_{IP3} points are -5 and 5 dBm, respectively at the output.

LNA is around -5 dBm which should result in a P_{IP3} of around +5 dBm (a rule of thumb [35]). The corresponding dynamic range for a 200 kHz channel is about 93 dB, while the spurious-free dynamic range is ~69 dB, which are comparable to the previously reported bipolar LNA results [30].

3.2.3 Errors from De-embedding of Conventional Open Pads

Due to substrate coupling, the circuit model in Figure 3-1 is not correct and the extracted R_s and C_{cap} have errors. To match the actual capacitors under test in the measurement system, the circuit model in Figure 3-1 must

be modified. Figure 3-11(a) shows the modified circuit model for one-port measurement. Since the p^+-substrate has a very low resistivity (<50 mΩ-cm), the p^+ substrate is modeled as a short in Figure 3-11(a). Because the p^+-substrate is not grounded at the back of the chip, signal must travel back to ground pad through Z_{pad} and $Z_{nw\text{-}psub}$ (Figure 3-11(a)). The total parasitic series resistance of the capacitor, and that between the p^+-substrate and bottom plate of

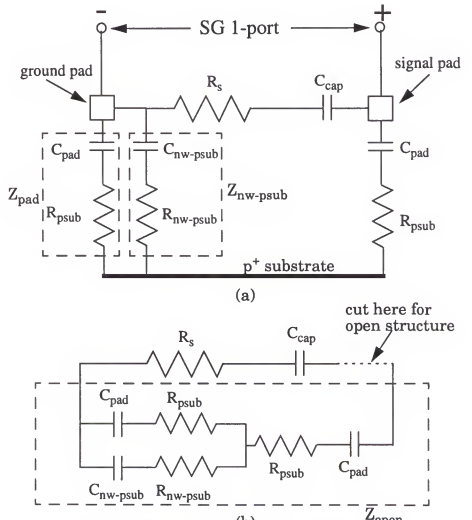


Figure 3-11 (a): Modified circuit model with substrate coupling for actual capacitors under test. (b) Rearrange of the circuit schematic in (a).

the capacitor are lumped into two single resistors R_s and $R_{nw\text{-}psub}$ for simplicity. For clarity, the circuit elements in Figure 3-11(a) are rearranged, and redrawn in Figure 3-11(b). It can be clearly seen that the proper open structure should be the same as the capacitor structure without the interconnect between pad and the top plate of the MOS capacitor (dotted line in Figure 3-11(b)). It is also good for characterizing the shunt parasitics $C_{nw\text{-}psub}$ and $R_{nw\text{-}psub}$ since C_{pad} and R_{psub} can be easily measured. The impedance of the new open structure (Z_{open}) to be de-embedded from the measured one-port data becomes

$$Z_{open} = Z_{pad} + \frac{1}{\frac{1}{Z_{pad}} + \frac{1}{Z_{nw-psub}}} \tag{3.4}$$

where

$$Z_{pad} = R_{psub} + \frac{1}{j\omega C_{pad}} \tag{3.5}$$

and

$$Z_{nw-psub} = R_{nw-psub} + \frac{1}{j\omega C_{nw-psub}} \tag{3.6}$$

while the impedance of the conventional open $Z_{conv\text{-}open}$ is $2 \cdot Z_{pad}$. Simulations using Matlab [36] show that this discrepancy results in an over estimate of parasitic series resistance R_s but a minor impact on the extracted MOS capacitance. Thus, the overall quality factor is under estimated using the simple open structure. Figure 3-12 shows MOS capacitances, parasitic series resistances, and quality factors plots using conventional open $Z_{conv\text{-}open}$ (sym-

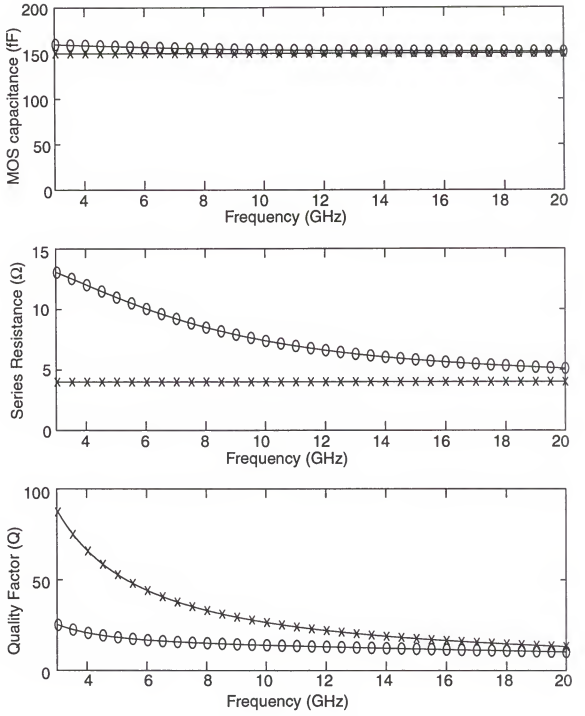


Figure 3-12 MOS capacitances, parasitic series resistances, and quality factors plots using conventional open $Z_{conv\text{-}open}$ (symbol 'o') and new open Z_{open} (symbol 'x') for de-embedding.

bol 'o') and new open Z_{open} (symbol 'x') for de-embedding. The extracted series resistance using the new open structure is essentially constant between 3 and 20 GHz. In this simulation, C_{cap}, R_s, $C_{nw\text{-}psub}$ and $R_{nw\text{-}psub}$ (Figure 3-11) were estimated from layout, and Z_{pad} were extracted from the measured S-parameters. These parameters were assumed to be frequency independent. As will be shown in section 3.2.5, the resistance versus frequency plot of a capacitor extracted using the new open structure is essentially flat over the measurement frequency range between 3 and 9-GHz in contrary to the strong frequency dependence for the resistance shown in Figure 3-12. The error between extracted and simulated model parameters is less than 20%.

Another potential approach to eliminate the error is to use a 2-port measurement structure [35]. Figure 3-13 shows a circuit model for the capaci-

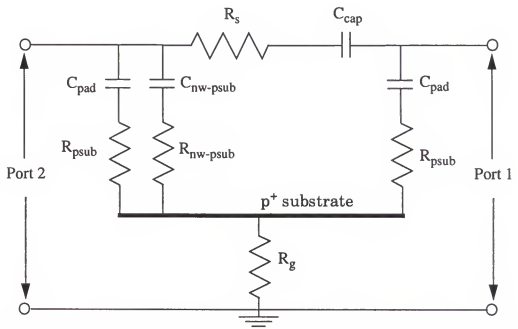


Figure 3-13 A circuit model of the capacitor test structure for 2-port measurement.

tor test structure. The resistor R_g represents the resistance between p^+-substrate and top-side p-substrate diffusions connected to ground pads. As can be seen from Figure 3-13, the admittance y_{12} (or y_{21}) consisting of R_s and C_{cap} can not be simply extracted from the 2-port S-parameter data [35]. Therefore, the one-port measurement with the improved open structure is preferred.

3.2.4 A Pad Structure with a Ground Shield

The difficulties of two-port measurement described in the previous section can be overcome if Z_{pad} is connected directly to ground instead of through p^+-substrate [37]. This can be accomplished by placing ground shields underneath the metal pads. Figure 3-14(a) shows a cross section of a pad with a ground shield and a circuit model with ground-shielded pads for 2-port measurements. R_{gs} is the resistance of ground shield which is typically on the order of a few ohms, $C_{pad\text{-}gs}$ is the capacitance between the metal pad and ground shield and $Z_{gs\text{-}psub}$ is the impedance between the ground shield and p^+-substrate. $Z_{gs\text{-}psub}$ in Figure 3-14(a) would be reduced to $R_{gs\text{-}psub}$ if the ground shield is laid out using p-substrate diffusion. From Figure 3-14(a), R_s and C_{cap} can be easily extracted from y_{12} (or y_{21}) data. For one-port measurement using ground-shielded pads, the circuit ground is directly connected to ground pad (signal pad of port 2 in Figure 3-14(a)) and thus, the components between ground pad and circuit ground can be eliminated. Figure 3-14(b) shows a circuit model for the one-port test structure. The complexity is greatly reduced compared to that in Figure 3-11(a).

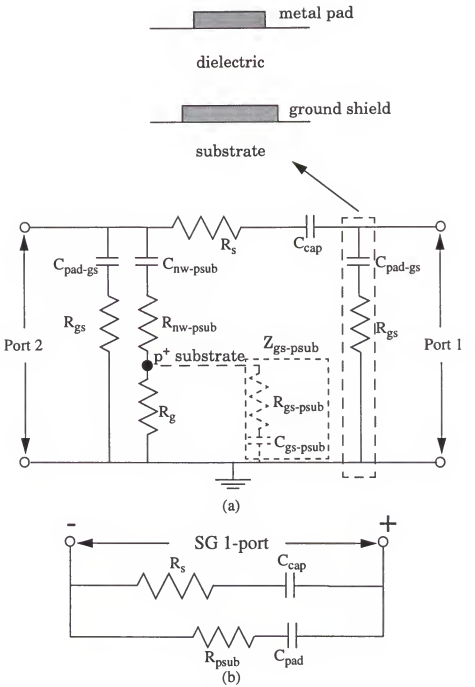


Figure 3-14 (a): A cross section of a ground-shielded pad and a circuit model of the capacitor test structure with a ground shield for 2-port measurements. (b): A circuit model with a ground shield for 1-port measurements.

3.2.5 MOS Capacitors for Varactor Applications

The voltage dependence of MOS capacitance discussed in the previous sections can be exploited to form a varactor. The transition between depletion and accumulation regions in the C-V plot has a voltage span of about 1.5 to 2 V which also makes the MOS varactor suitable for low-voltage operation. The possibility of achieving high quality factor at high frequencies is further attractive. Two MOS varactors using two advanced CMOS processes are demonstrated. VCOs utilizing these two MOS varactors are described in CHAPTER 4. One of the varactors is implemented in a 0.25-μm digital CMOS process for 5.5-GHz ISM band applications while the other is implemented in a 0.1-μm bulk CMOS process which uses a 0.35-μm design rule set for >20-GHz operation. The maximum quality factor that can be achieved with an MOS varactor using the 0.25-μm CMOS process is also compared with that for a pn-junction varactor (section 3.3.2). The maximum Q for an MOS varactor is much higher.

A C-V plot of an MOS varactor implemented in the 0.25-μm CMOS process is shown in Figure 3-15. When the bias voltage is greater than ~0.5 V, the MOS varactor is operating in accumulation region. Although not significant, the capacitance decreases with voltage when the bias condition is >2 V. This is due to the polysilicon gate depletion effect [38], [39], [40], [41]. Between -1 and 0.5 V, the capacitance increases with bias voltage. This is the region in which the structure can be used as a varactor. Compared to the C-V characteristic of a pn-junction varactor (in the next section), the transition of an MOS varactor

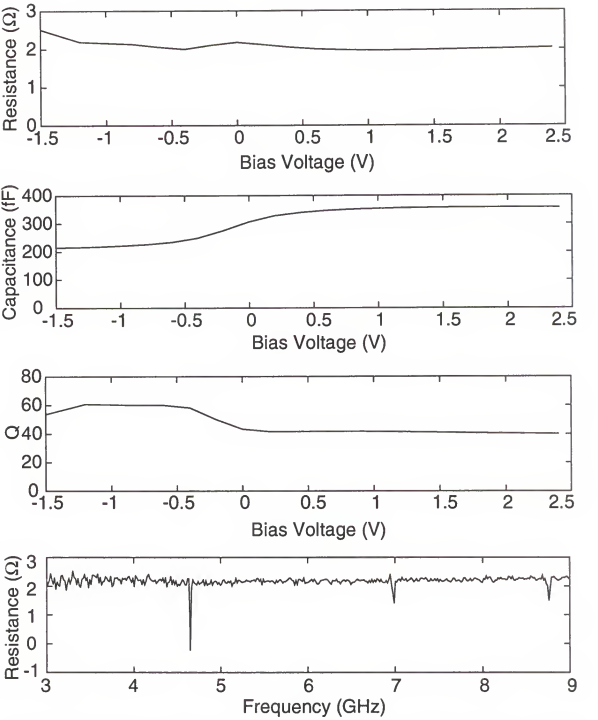


Figure 3-15 R_s, C_{cap}, and Q versus gate bias plots of the MOS varactor implemented in the 0.25-μm CMOS process, and a resistance versus frequency plot at -1-V gate bias.

is much more linear. The linearity of the transition is another advantage of using MOS varactors. A voltage-controlled oscillator (VCO) using this MOS varactor has more linear frequency tuning characteristic, which is preferred. The varactor is in depletion region below -1.5 V. The resistance and Q versus gate bias voltage plots are also shown in Figure 3-15. The highest and lowest Q are ~60 and ~40 at 5.5 GHz, respectively. A resistance versus frequency plot at -1-V gate bias is also shown in Figure 3-15 which is essentially flat over the whole frequency range. Q of ~60 is not the best that can be achieved in this process. Another test structure shows that Q of 140 (Figure 3-16) at 5.5 GHz is achievable. As will be shown in the next section, Q of 140 at 5.5 GHz is much

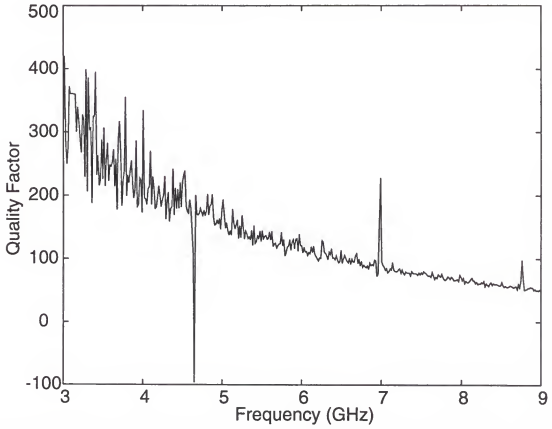


Figure 3-16 A Q versus frequency plot of an MOS varactor. The Q is ~140 at 5.5 GHz.

greater than that can be achieved using a pn-junction varactor (diode array). Although an MOS capacitor is a good candidate for varactor application, the voltage dependence in the accumulation region is problematic since a phase locked loop system (PLL) needs a VCO with a monotonic tuning characteristic.

Figure 3-17 shows a C-V plot for an MOS capacitor implemented in the 0.1-μm bulk CMOS process. The C-V characteristic is the same as that shown in section 3.2.2 except the frequency-dependent capacitance at >0.4-V gate bias. This is due to the polysilicon gate depletion effect [38], [39], [40], [41], which also decreases the maximum capacitance. The polysilicon depletion effect is important when the gate oxide thickness is small and the amount of

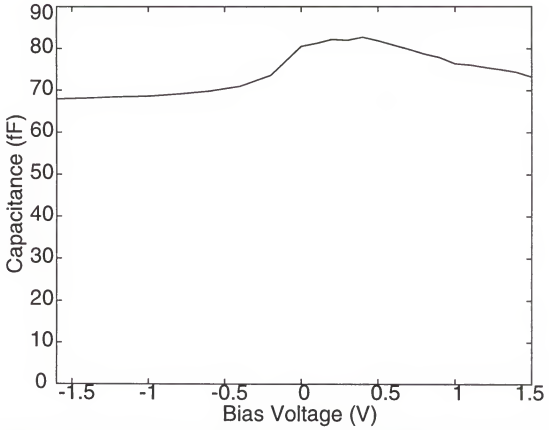


Figure 3-17 A C-V plot for an MOS capacitor implemented in a 0.1-μm bulk CMOS process.

dopants in the gate polysilicon is not enough such that the thickness of the depletion layer formed in the gate material is comparable to the gate oxide thickness. The gate oxide thickness of the 0.25-μm CMOS process is ~58 angstrom while that of the 0.1-μm CMOS process is ~30 angstrom. Hence, the polysilicon depletion effect in the 0.1-μm CMOS process is more significant than that in the 0.25-μm process. The measured quality factor of the 0.1-μm bulk CMOS process is shown in Figure 3-18. Due to larger overlap and fringing capacitances, the capacitance ratio between maximum and minimum capacitances in the C-V plot is smaller than that described in section 3.2.2. Ground-shielded pads are used for the test structure so that the parameter extraction is accurate. At 26 GHz, the varactor has a minimum Q of ~20 which is excellent. From Eq. 3.2, the series resistance of an MOS capacitor can be

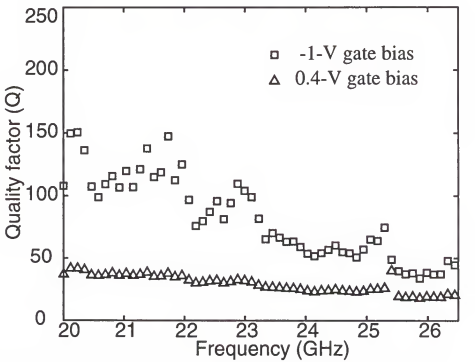


Figure 3-18 Q versus frequency plots for gate biases of 0.4 and -1 V.

very small when minimum L and W (0.1 and 1.7 μm, respectively in this case) are used. Thus, the ultimate limiting factor of the quality factor is the metal interconnect and contact and via resistances. Since Q of 20 is not achievable for a pn-junction varactor at >20 GHz, it is necessary to utilize an MOS varactor for VCO applications. To handle the polysilicon gate depletion effect, the gate bias voltage range of the MOS varactor should be limited.

3.3 High-Q P-N-Junction Varactors

3.3.1 Motivation

For an LC voltage-controlled oscillator operating around 1 and 5 GHz with an integrated LC tank, the quality factor of the LC-network is typically dominated by the inductor-Q. The total Q of an LC tank is approximately equal to $1/\left(\frac{1}{Q_L}+\frac{1}{Q_C}\right)$ where Q_L and Q_C are the Q factors of the inductor and capacitor, respectively. According to this, in order to reduce the overall Q degradation by less than 10% from the Q_L, Q_C must be more than 9 times higher than Q_L. In addition, it is desired to have a monotonic C-V characteristic from a varactor. These reveal the need for a high-Q pn-junction varactor.

3.3.2 Varactors Implemented Using Diode Arrays

Figure 3-19 shows a partial layout of a pn-junction varactor. The p^+ diffusion is surrounded by n-well ties and all cells are connected in parallel. The

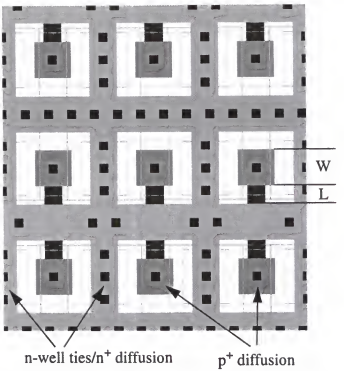


Figure 3-19 A partial layout of the p^+-to-n-well junction diode.

capacitance is from the bottom and side walls of the p^+-to-n-well junction while the parasitic series resistance is from the n-well resistance between p^+ and n^+ diffusions as well as contact and metal series resistances. The resistance and Q can be approximated as [8], [42]

$$R_{var} = \left(R_{nw,\square} \times \frac{2 \cdot L}{L + 2 \cdot W} \times \frac{1}{4} + \frac{R_{nw,\square}}{28.6}\right) \times \frac{1}{N} \tag{3.7}$$

and

$$Q_{var} = \frac{1}{\omega R_{var} C_{var}} = \frac{1}{\omega C_{var}} \cdot \frac{N}{R_{nw,\square}} \cdot \frac{15.3 \cdot L + 2 \cdot W}{28.6 \cdot (L + 2 \cdot W)}, \tag{3.8}$$

where L is the spacing between p^+ and n^+ diffusions, W is the width of p^+ diffusion, N is the number of cells, $R_{nw,\square}$ is the sheet resistance of n-well and

C_{var} is the desired capacitance. In order to reduce the series resistance, N should be as large as possible for a given capacitance resulting in W to be as small as possible. L should also be as small as possible from Eq. 3.7. Hence, the maximum Q can be achieved by minimizing the sizes of p^+ diffusions and p^+-to-n^+ spacing. The measured Q of a varactor implemented in a 0.8-μm CMOS process at 0 V bias (low-Q condition) is shown in Figure 3-20 (symbol 'x'). L, W and Q at 1.1 GHz are 1.6 μm, 3.2 μm and 24, respectively. The Q is not the best that can be achieved in this process since the width of the p^+ diffusion is not minimized. Decreasing the p^+ diffusion width will however increase the varactor area.

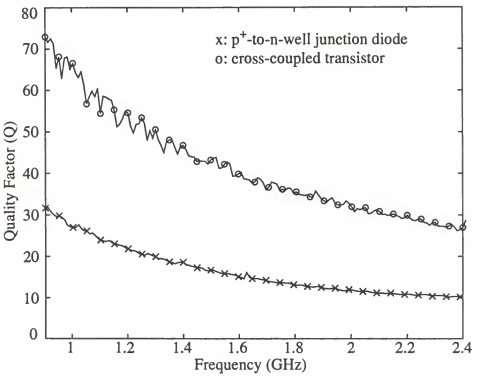


Figure 3-20 Quality factor versus frequency plots for the p^+-to-n-well junction diode at 0-V bias (symbol 'x') and the drain-to-body parasitic capacitance of the cross-coupled transistor (symbol 'o'). The Q's are 24 and ~57 at 1.1 GHz for the diode and transistor, respectively.

Another pn-junction varactor using minimum L and W was implemented in a 0.25-μm standard digital CMOS process. The spacing L and width W are both 0.6 μm (the minimum dimensions in this process). The measured quality factor is ~57 at 5.5 GHz (Figure 3-21) when the bias voltage is 0 V (the worst condition). This is the highest Q that can be achieved in this process. Unlike the pn-junction varactor implemented in a 0.8-μm CMOS process, the limiting factors for the quality factor in a 0.25-μm CMOS process are not only the n-well resistance but also the contact and silicide resistances. This is due to the fact that as the technology is scaled down, the p^+-diffusion width (W) and the n-well sheet resistance are decreased, but the contact resistance

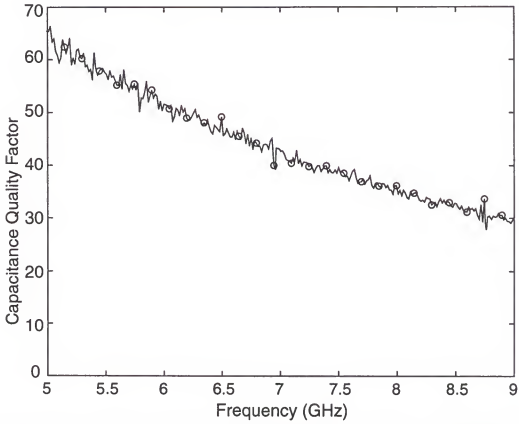


Figure 3-21 Quality factor of the pn-junction varactor implemented in a 0.25-μm CMOS process. The bias condition is 0 V.

increases. Also, the number of contacts for the p^+ diffusion area is limited to 1 (to have a minimum W). Hence, the ultimate limitations are the n-well and contact resistances. This is different from that of an MOS varactor whose ultimate limitation is the metal interconnect resistance which is much smaller than the n-well, and contact resistances. The series resistance of a pn-junction varactor limits its usability at very high frequencies. The error between extracted and simulated model parameters is less than 10%.

3.4 Optimizations of Transistor Layout

For applications such as voltage controlled oscillators which require a high-Q LC network, not only the quality factors of the inductor and varactor but also the parasitic capacitance of transistors connected to the LC-tank need to be high. The loss for the parasitic capacitances of a transistor is mainly due to the substrate resistances between source/drain diffusions and substrate contacts (C_{db}, C_{sb}), and that between gate and substrate contacts (C_{gb}) when the transistor is off. Through a layout optimization, the substrate resistance can be reduced and thus the quality factor of C_{db}/C_{sb} and C_{gb} can be improved. Figure 3-22 shows a partial layout of a cross-coupled PMOS transistor. The transistor is broken into small cells and each cell is surrounded by n-well contacts. With this layout, the effective parasitic series resistances between the drain and n-well ties, and that between polysilicon gate and n-well ties can be reduced. The parasitic resistance due to the polysilicon gate (R_{poly}) is also minimized at the same time. The penalty of this layout optimization is once

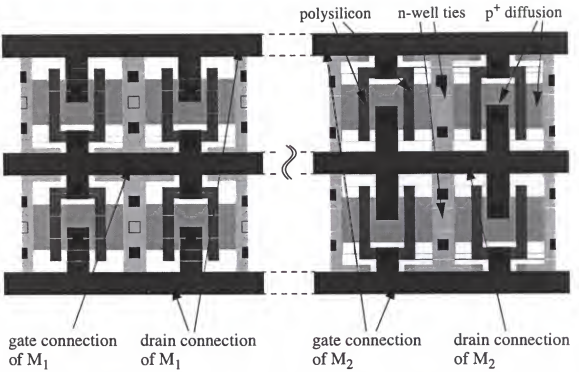


Figure 3-22 A partial layout of the cross-coupled PMOS transistor. The source diffusions are shorted to n-well ties using the silicide to reduce the layout area.

again a larger area for the transistors. However, due to the availability of silicide in most sub-micron processes, the source contacts can be eliminated and the source diffusion is connected to the surrounding n-well ties by silicide to reduce the total area (if the source terminals were designed to be shorted to the body terminals). As will be shown in CHAPTER 4, for VCOs, most of the die area is consumed by on-chip inductors, and the area penalty associated with the transistor optimization is insignificant. When multiple fingers of relatively narrow transistor channel width are used, the width reduction due to process biases (delta W) should be included in simulation. A measured Q versus frequency plot for the C_{db} of a 400-μm wide and 0.8-μm long PMOS transistor implemented in a 0.8-μm CMOS process is shown in Figure 3-20

(symbol 'o'). The Q factor at 1.1 GHz is ~57, which is high. Extra metal 2 and 3 are used to reduce the total interconnect resistance.

Another benefit using this layout is the symmetry of the cross connection between M1 and M2 (Figure 2-3). Since the metal connections for gate and drain of a transistor are in parallel and next to each other (Figure 3-22), the gate connection of M1 (M2) can be horizontally aligned to the drain connection of M2 (M1). This avoids a cross connection in different metal layers which would induce a mismatch in capacitance.

3.5 On-Chip Spiral Inductors

As mentioned earlier, the quality factor of an LC-tank is crucial to VCO design. Especially for frequencies below ~10 GHz, the inductor Q is typically much smaller than those of other passive components, the inductor design becomes the determining factor of the VCO performance. However, due to the lossy silicon substrate and the metal resistance, it is difficult to achieve a high quality factor.

An accurate modeling of an on-chip spiral inductor requires 3-D electromagnetic (EM) simulations which are time consuming. To speed up the inductor design process, simplified models as well as guidelines to improve the inductor characteristics have been intensively studied and proposed [16], [29], [37], [43], [44], [45]. The results are summarized in the following:

1. The conventional definition of quality factor (Q_{conv}), Im(Z)/Re(Z) where Z is the input impedance of an inductor, is not correct at high frequen-

cies where the energy stored in the parasitic capacitance is comparable to that stored in the inductor [16]. Inductor optimization using Q_{conv} could lead to improper optimization of inductors. A Q definition using half-bandwidth method (Q_{bw}) [16] should be used for inductor design.

2. To reduce the parasitic capacitance and thus increasing the overall Q, it is desired to have a minimum spacing between metal traces because the positive mutual inductance can be maximized minimizing the total metal area and parasitic capacitance. However, due to the proximity effect [37], the effective series resistance is increased at high frequencies and the overall Q is decreased. From experiments [46], for a typical inductor having a ~6-μm-wide metal line and operating at a few GHz, ~2-μm of spacing results in a good combination of inductance, series resistance and parasitic capacitance improving the overall Q. Hence, the metal spacing is typically chosen to be >1/3 of the metal width for inductors operating in GHz range.
3. From a 3-D EM simulation, the magnetic field is stronger at the center of a spiral inductor [44]. If a spiral inductor is filled all the way to its center, the strong magnetic field at the center would induce large eddy current in the inner turns, thus increasing the effective resistance in the inner turns [44]. The net effect is that the inner turns contribute less inductance but larger resistance, which suggests that the inductor should be hollow at its center.

4. From the magnetic field pattern, an inductor with larger area would induce larger eddy current in the substrate [44]. Since the magnetic field induced by the eddy current is opposite to that of the inductor, the inductance is decreased. In addition, the substrate acts like a transformer (Figure 3-23), the loss associated with the substrate resistance would show up as an increase of the effective series resistance. The overall Q of the inductor can thus be significantly degraded. Two inductors were experimented using a 0.25-μm CMOS process [47]. One has an area of ~90x90 μm^2 while that for the second is ~110x110 μm^2. The inductors were fabricated on both ~8-Ω-cm p^- and ~0.01-Ω-cm p^+ (with p^- epitaxial) substrates. Q of the inductor with an area of ~90x90 μm^2

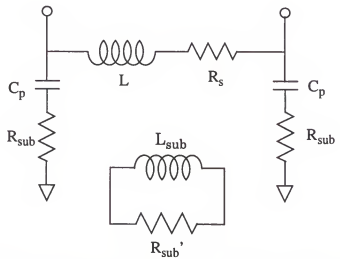


Figure 3-23 A simple model of the substrate effect. L is the inductance, R_s is the series resistance, C_p is the shunt parasitic capacitance between metal and substrate, R_{sub} is the substrate resistance seen by the inductor, L_{sub} is the equivalent inductance associated with the eddy current and R_{sub}' is the resistance seen by the eddy current. L and L_{sub} act as a transformer.

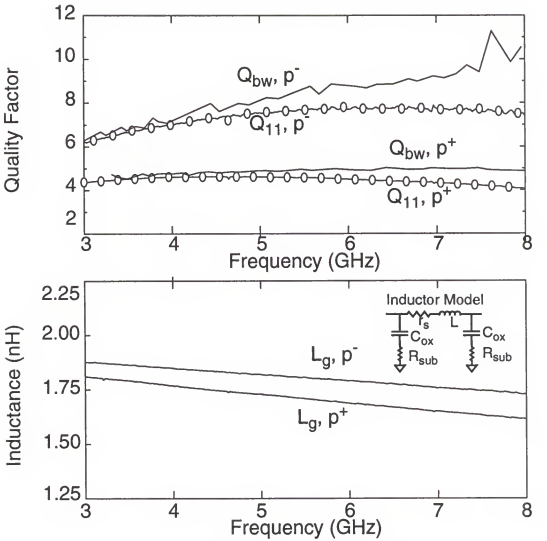


Figure 3-24 Inductances and quality factors for the larger inductor in p^+ and p^- substrate.

on the p^+ substrate is degraded by ~29% compared to that on a p^- substrate while the larger inductor is degraded by ~50% (Figure 3-24). The area of an inductor should be limited. These results also indicate that a p^- substrate is preferred for on-chip spiral inductors.

5. One of the factors degrading inductor Q is the substrate resistance (R_{sub}) which is defined as the parasitic resistance in series with the

shunt capacitance. When R_{sub} is low, Q of C_p becomes high since C_p is approaching an ideal capacitor having no effect on the inductor Q. For very high R_{sub}, the shunt parasitics approach open and once again would have no effect on the inductor Q. An inductor Q versus R_{sub} plot is shown in Figure 3-25. Since it is not possible to substantially increase the substrate resistance for a given process technology, the substrate resistance is typically made small by having a ground shield underneath the inductor [43], [48]. The penalty is higher C_p which reduces the self-resonant frequency. To avoid inducing eddy current in the ground shield, the shield is patterned such that the eddy current can not be formed. A typical layout of a patterned-ground-shield (PGS)

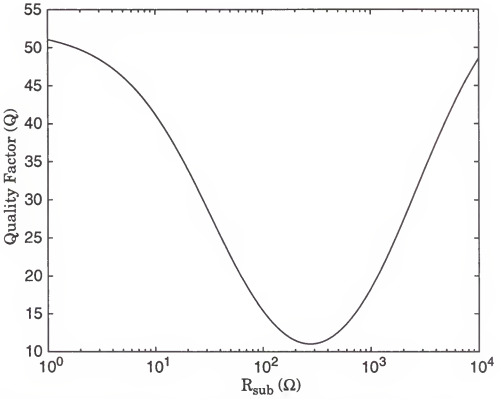


Figure 3-25 A quality factor versus substrate resistance (R_{sub}) plot.

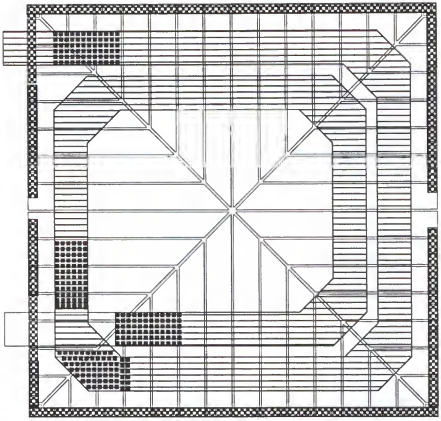


Figure 3-26 A typical layout of a patterned-ground-shield inductor.

inductor is shown in Figure 3-26. The metal connection of the PGS should not form a closed loop surrounding the inductor. The spacing between the ground shield stripes should not be minimum to reduce the capacitive coupling which could form a eddy current path.

Although it is difficult to simulate an inductor, a simplified model has been developed to estimate the inductor parameters. The substrate effect which is difficult to simulate without using a 3-D simulator is not taken into account but may be reduced by having a smaller inductor area [44]. The inductance, L, of a spiral inductor is estimated using the Greenhouse formula [49]. The substrate resistance, R_{sub}, is estimated using the sheet resistance of the

ground shield layer and the measured data from various CMOS processes. The series resistance, R_s, can be approximated by simply taking the corners and total number of squares of the metal into account when the turn spacing is larger than ~1/3 of the metal width. Although the larger (than the minimum metal spacing) turn spacing decreases the inductance/area, it would result in a better combination of R_s and C_p for higher overall inductor Q. Modeling of the parasitic shunt capacitance, C_p, is very complicated and again requires a 3-D simulator for exact capacitance values. The typical models and capacitance look-up tables from the providers of CMOS processes do not have the exact conditions for conductors in an inductor, which has open on the top and conductors at the bottom, conductors on both top and bottom, or conductors on the top and a ground plane at the bottom. A simplified and effective model is developed [50] to alleviate the cumbersome and time consuming procedure using a 3-D simulator. It has been implemented in Matlab [36], and only needs a few seconds to estimate C_p, R_s and R_{sub}, and the bandwidth Q [16] of an inductor.

Figure 3-27 shows an example cross section of a 2-turn spiral inductor with 2 metal layers connected in parallel. The capacitance components being taken into account are also shown in this figure. The fringing and area capacitances are denoted as C_{fringe} and C_{area}. The fringing capacitance between turns is neglected because the turn spacing is typically small compared to the metal width. The coupling capacitance between turns is also neglected since the conductors between adjacent turns are approximately at the same poten-

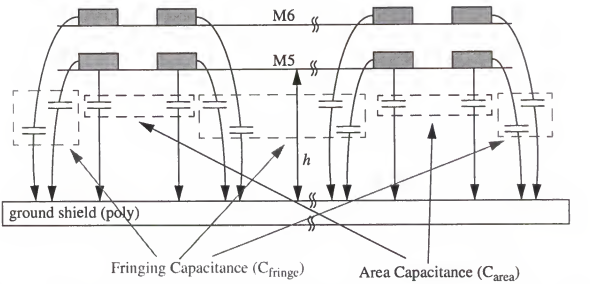


Figure 3-27 An example cross section of a spiral inductor with 2 turns. The capacitance components being taken into account are also shown.

tial. Since the inner turn contributes less inductance and more resistance especially when the distance between the inner edges of the inner turn is small, inductors are typically designed to have a large hollow (relative to the metal width) at the center. Hence, the fringing capacitance of the inner edges of the inner turn are taken into account together with the outer edges of the outer turn. The fringing capacitance per side is approximated using a modified model from [8] and is

$$C_{fring} = \left[\frac{2\pi}{\ln\left\{1 + \frac{2h}{t} + \sqrt{\frac{2h}{t}\left[\frac{2h}{t} + 2\right]}\right\}} - \frac{\frac{t}{2}}{h} \right] \tag{3.11}$$

where t is the total metal thickness and h is the height of the insulator between the lower-level metal and ground shield (Figure 3-27). Finally, the area capacitance between the lower-level metal and ground shield is calcu-

lated and C_p is derived by adding C_{area} and C_{fringe}. The difference between the simulated and the measured C_p is less than ~10% which is acceptable.

3.6 Summary

MOS capacitors with an extrapolated Q-factor over 100 at 900 MHz were demonstrated using a conventional foundry CMOS process. Since the intrinsic capacitance is high and the MOS structures are naturally available in CMOS processes, the capacitors are area-efficient and inexpensive. Using the MOS capacitors, a low noise amplifier with a -5-dBm P_{1dB} compression point and an estimated P_{IP3} of around 5 dBm at the output was demonstrated [34]. This suggests that despite the concerns for non-linearity and parasitic capacitances, the simple and inexpensive MOS capacitors should be suitable for many RF applications such as bypassing, matching, coupling as well as frequency tuning in VCOs. In addition, if the bias and operating range are properly restricted, the structure can also be used as a linear capacitor. Due to the high-Q and the voltage-dependent capacitance (C-V) characteristics, an MOS capacitor is an obvious candidate for low-voltage varactor applications. Using the MOS structure, at high-Q bias conditions, Q of 140 at 5.5 GHz in a 0.25-μm CMOS process and Q of 40 at 26 GHz in a 0.1-μm CMOS process are possible. The quality factors at low-Q conditions for the 0.25 and 0.1-μm processes are 73 at 5.5 GHz and 20 at 26 GHz, respectively. Although the Q is high, polysilicon depletion effect must be taken into account when designing VCOs.

Varactors implemented using a p^+-to-n-well diode array in a bulk CMOS process was investigated. The Q at 1.1 GHz and 0-V bias (worst case) is ~24. This quality factor can be increased by decreasing the p^+ diffusion size. As will be discussed in CHAPTER 4, this varactor is used in VCOs to achieve excellent phase noise characteristics. By optimizing the structure in a 0.25-μm standard digital CMOS process, Q of ~57 has been achieved at 5.5 GHz and 0-V bias. Using the same optimization technique for the pn-junction varactors, Q of the parasitic capacitances, C_{db}, C_{sb} and C_{gb}, associated with the cross-coupled transistors in a VCO can be improved. The measured Q at 1.1 GHz and 0-V bias is ~57 in a 0.8-μm CMOS process. Since the channel width for each finger is small, width reduction due to the fabrication process bias needs to be taken into account in layout.

Lastly, guidelines for designing on-chip spiral inductors are summarized. A simplified and efficient model for the inductor simulation was developed. A Matlab [36] routine was also created to facilitate rapid inductor design. The quality factors of spiral inductors with a PGS have been measured on both p^+ and p^- substrates in a 0.25-μm CMOS process. Q is higher on p^- substrates. The PGS does not significantly reduce the Q degradation from the eddy current effects. The development of high-Q passive components on CMOS processes and the insights gained from the work was the foundation for the development of low-power and low-phase-noise CMOS integrated phase-locked loop circuits which are presented in the following chapters.

CHAPTER 4
VOLTAGE-CONTROLLED OSCILLATORS

4.1 Introduction

A voltage-controlled oscillator (VCO) is one of the most important building blocks in a phase-locked loop frequency synthesizer system because its phase noise performance determines the spectral purity of the synthesizer outside the loop bandwidth which is part of the requirements in wireless communication systems. Due to finite quality factors of on-chip inductors, varactors and (parasitic) capacitors, it is very difficult to achieve low power and low phase noise with an integrated VCO. Furthermore, owing to inherent nonlinearity of devices, the analysis using a linearized model has limited meaning. In this chapter, LC-VCOs operating at 900 MHz, 5.5 GHz, and >20 GHz designed using the guidelines discussed in CHAPTER 2 are described. These VCOs use a modified differential circuit schematic to reduce the phase noise contributed by the bias circuit. For the two 900-MHz VCOs, one uses only integrated patterned-ground-shield (PGS) inductors [43] while the other uses a combination of a PGS inductor, and bondwires and package leads to increase Q of the LC resonator. The phase noise performance for both VCOs exceeds the GSM specifications according to [52]. The VCOs designed for 5.5 GHz and >20 GHz have also been fabricated and measured. The phase noise perfor-

mance of the 5.5-GHz VCOs is the lowest reported when published. The advantages and disadvantages of using diode arrays and MOS capacitors as varactors are discussed. The >20-GHz VCOs have the highest frequencies of operation from a CMOS process to date. The measured frequency tuning characteristic raises some potential problems to be taken care of when designing a VCO using an advanced CMOS process. Another VCO using a differential ring (relaxation) oscillator structure is also demonstrated. This VCO works at ~9.7 GHz.

4.2 A 1.24-GHz Monolithic PMOS LC-VCO

Satisfying the GSM phase noise requirement for a CMOS VCO [52] has been a major challenge. Especially for the original GSM system operating near 1 GHz, this has been problematic because the inductor Q is lower and the required signal to noise ratio is 3 dB higher than that of the DCS1800 [52], [53], [54]. In this section, a 1.24-GHz monolithic CMOS VCO with phase noise at 10-kHz, 600-kHz and 3-MHz offsets of -88 dBc/Hz, -125 dBc/Hz and -137 dBc/Hz, respectively (the oscillation frequency = 1.28 GHz) is demonstrated [51]. The best 1-GHz CMOS VCO before this work is the one implemented in a 0.4-μm CMOS process with measured phase noise of -108 dBc/Hz at an offset of 100 kHz and extrapolated phase noise of -123.5 dBc/Hz at an offset of 600 kHz [52]. The excellent phase noise performance of this VCO was achieved despite the use of an integrated inductor with a low Q-factor of 3.5. The VCO is fabricated in a low-cost 5-Volt 0.8-μm foundry CMOS process with three

metal layers. The process uses p^+ substrates with a p^- epitaxial layer and this exacerbates the low Q factor problem of on-chip inductors [45]. The VCO exclusively uses buried channel PMOS transistors for lower 1/f noise (CHAPTER 2) and PGS integrated spiral inductors in the LC tanks for higher Q. The VCO was mounted in an SOIC like package for test. This is the first CMOS VCO for 1-GHz applications to have measured phase noise which exceed the GSM specifications at both 600-kHz and 3-MHz offsets of less than -121 dBc/Hz [52] and -135 dBc/Hz, respectively.

4.2.1 Design Considerations

In MOS transistors, mobility and carrier number fluctuations result in high flicker (1/f) noise (CHAPTER 2), which poses problems for attaining low close-in phase noise in CMOS VCO's. Measurements have shown that the input-referred 1/f noise for a buried channel PMOS transistor from the 0.8-μm CMOS process at saturation region of operation can be more than one order of magnitude lower than that of an NMOS transistor with the same width CHAPTER 2). If only buried channel PMOS transistors are used in a VCO and the transconductance, G_m, is kept the same as that of NMOS transistors for a given current by adjusting the channel width, the phase noise within $1/f^3$ region (due to 1/f noise) should be smaller.

Figure 4-1 shows the VCO circuit schematic including buffers. The g_m of the cross coupled transistors, M1 and M2, was chosen to be 10 mS at V_{DD}=3 V to provide sufficient negative resistance to cancel the loss in the LC-resona-

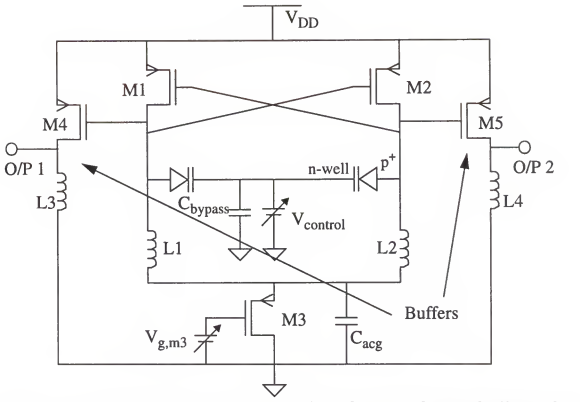


Figure 4-1 A circuit schematic of the LC-oscillator including buffers. The VCO exclusively uses buried channel PMOS transistors with low 1/f noise for improved phase noise performance.

tor. Instead of an NMOS current source, a PMOS transistor, M3, is placed at the bottom to perform a comparable function. This configuration allows the VCO core output to be dc coupled to the buffer while maintaining the flexibility for setting the gate bias voltage of the buffer transistors (M4 and M5) without using an NMOS transistor with higher 1/f noise. The dc level at the output of the VCO core has lower sensitivity/gain (verified by Spice) to the noise at the gate of M3 (a source follower with a low gain) compared to the topology with a conventional NMOS current source at the bottom which is essentially a common source amplifier with a higher gain. Hence, the noise in the tail current, which may be converted into phase noise [23], [24] can be reduced. This

lowers sensitivity to the noise at the gate of M3, and also decreases the noise in the junction voltage and fluctuation of the capacitance of the tuning diodes, which reduces the FM noise at the outputs of a VCO core. Thus, the lower conversion gain for the noise from a bias circuit and not having an additional bias circuit for the buffer [55] should decrease the total phase noise. The buffer is a PMOS common-source amplifier with an inductive load (13 nH) which can provide a larger and more symmetric swing to the 50-Ω load than that from a resistively loaded buffer. The transistor width was chosen to be as large (100 μm) as possible to increase the output power while making sure that it is not too large such that the parasitic capacitance of the transistor does not significantly decrease the tuning range. The output dc level is close to 0 volt, so that the output signal can be directly connected to a spectrum analyzer.

The inductors for the LC-tank are implemented using a PGS inductor [43] which was optimized using Q factors estimated with the half-band-width method [16], [48]. The inductance of L1 and L2 was chosen to be ~4 nH. It was determined that the highest Q can be achieved when shunted metal 2 and 3 layers are used for the inductor trace. The area of the inductor is 400x400 μm^2. The metal spacing and width, and number of turns are 2 μm, 38 μm, and 3, respectively. The estimated parasitic capacitance seen looking into the inductors is 1.5 pF.

The cross-coupled transistors are laid out in such a way to reduce the parasitic substrate resistances for the gate-to-body (C_{gb}) and drain-to-body (C_{db}) capacitances in order to improve the Q of the overall resonator (section

3.4). The sources are shorted to n-well ties using a silicide layer to reduce the total transistor area. The Q of the capacitances at the drain nodes of M1 and M2 are limited by the substrate resistance associated with the C_{db} and C_{gb}. A Q of ~53 at 1.2 GHz and 0-V bias for C_{db} was measured (section 3.4). To obtain an oscillation frequency of 1.16 GHz with the 4-nH inductance and 1.5 pF inductor parasitic capacitance, the sum of the varactor and transistor parasitic capacitances should be ~3.1 pF. The input capacitance of M1 and M2 ($C_{gs}+C_{gd}+C_{db}$) is ~0.9 pF, while that of the buffer transistor is ~0.2 pF. These leave ~2.1 pF for the varactor. The varactor is implemented using an array of p^+-to-n-well junction diodes and the capacitance is controlled by varying the n-well voltage. The n-well node is bypassed to ground using a 20-pF medium-Q MOS capacitor (section 3.2). The measured Q of the varactor is ~22 at 1.2 GHz and 0 V reverse bias (worst case).

4.2.2 Experimental Results and Discussion

The measured inductance of the PGS inductor is ~2.8 nH and the measured Q is 3.5 at 1 GHz, which is significantly lower than the design value of 7. The inductor was designed neglecting the effects of p^+ substrate [43]. Hence, the area of the inductor and the width of the metal trace were too large. These cause the magnetic field to penetrate deeper and larger eddy current induced in the p^+ substrate. This eddy current, in turn, reduced the total energy storage and decreased the effective inductance. To shield the magnetic

field from the p^+ substrate, eddy current should be induced in the ground shield. However, since the patterned ground shield (PGS) is specifically designed so that eddy current is not induced, the PGS is not effective in reducing the eddy current effects in the p^+ substrate and thus, the actual Q of the spiral inductor is lower than the design. This Q reduction also increases the power consumption for the VCO core. The spiral inductor design should have included the substrate effects.

Due to the lower Q of the inductors L1 and L2 than expected, the gate voltage of M3 is lowered to increase the bias current. Figure 4-2 shows an single-ended output spectrum with a 100-kHz span and a resolution bandwidth of 1 kHz. The power at the 1.28-GHz center frequency is -12.83 dBm. The phase noise at a 10-kHz offset is -88 dBc/Hz. To measure the phase noise at 600-kHz and 3-MHz offsets, an external amplifier with 20-dB gain, 5.5-dB noise figure, and 25-dBm P_{1dB} is connected at the output. A resulting single-side-band spectrum between 600-kHz and 3-MHz offsets from the center frequency is shown in Figure 4-3. The phase noise is -125 and -137 dBc/Hz at 600-kHz and 3-MHz offsets, which exceed the GSM requirements of less than -121 [52] and -135 dBc/Hz, respectively. Since these measurements include the noise of the measurement environment and those added by the amplifier, the actual phase noise should be even lower than reported here.

The center frequency is higher than the design due to errors in estimating the varactor capacitance and inductance of L1 and L2. The VCO core consumes 22 mA from a 3-V power supply. The tuning range is ~130 MHz for the

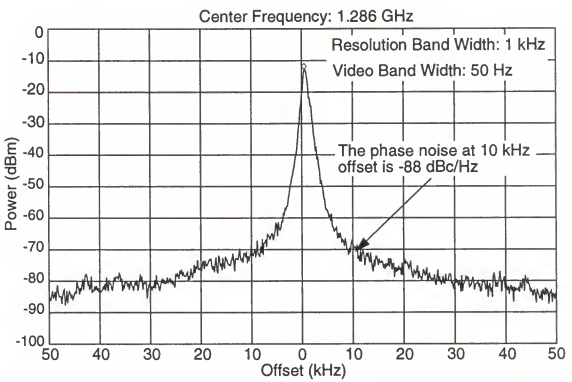


Figure 4-2 A 100-kHz span output spectrum (I_{vco}=18.8 mA, $V_{control}$=3V). The power at the 1.28 GHz center frequency is -12.83 dBm. The phase noise at a 10-kHz offset is -88 dBc/Hz.

control voltages between 0.5 and 3V. A frequency versus the control voltage plot is shown in Figure 4-4. Between 1.19 and 1.28 GHz (~90 MHz), the phase noise specification of -135 dBc/Hz at a 3-MHz offset is satisfied. Below 1.19 GHz, the phase noise measurements are limited by the noise floor of the measurement set-up due to a decrease of the signal power level. The minimum bias current from a 3-V supply for oscillation at 1.28 GHz while still satisfying the phase noise requirement is 17 mA.

Figure 4-5 is a die photograph of the VCO. The die size is 1.2x0.9 mm^2. A significant portion of the die is occupied by the inductors. All bond pads have a polysilicon ground shield underneath to reduce the substrate coupling.

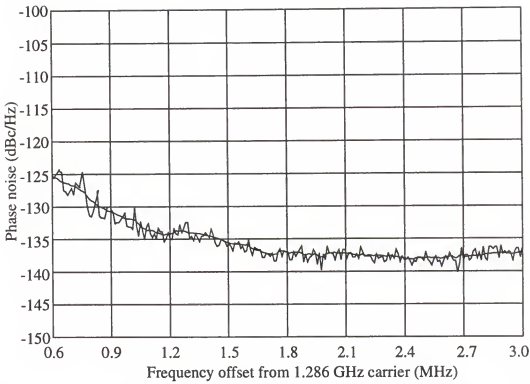


Figure 4-3 A single-side-band phase noise plot (I_{vco}=22 mA, $V_{control}$=3V). The phase noise is -125 and -137 dBc/Hz at 600-kHz and 3-MHz offsets. These exceed the GSM requirements of less than -121 [52] and -135 dBc/Hz, respectively.

Empty space in the circuit is filled in with p^+-substrate contacts to reduce the substrate coupling.

4.3 A 1.1-GHz Packaged PMOS LC-VCO

The VCO presented in the previous section has a very high power consumption of 66 mW at V_{DD}=3 V because of the low quality factor of the PGS inductor. As discussed, this is due to the extra power loss in the substrate. To overcome this problem, the inductor of the LC-resonator is formed using a series combination of an on-chip PGS [43] spiral inductor, bondwires and

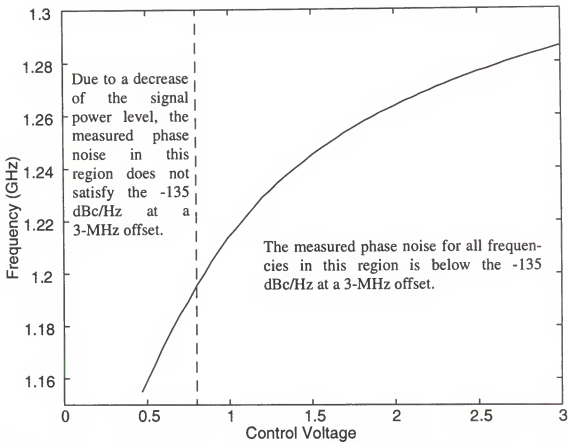


Figure 4-4 A frequency versus control voltage plot. The tuning range is ~130 MHz for the control voltages between 0.5 and 3V. Between 1.19 and 1.28 GHz (~90 MHz), the phase noise specification of -135 dBc/Hz at a 3-MHz offset is satisfied.

package leads [56]. This approach does not require extra board space beyond that required for the package leads. The packaged PMOS LC-VCO has a tuned frequency of 1.1 GHz and consumes only 12.7 mW at V_{DD}=2.7 V while achieving superior phase noise performance than the version demonstrated in section 4.2. With V_{DD}=2.7 V, the phase noise at 10-kHz, 100-kHz and 600-kHz offsets are -92, -112 and -126 dBc/Hz, respectively. The extrapolated phase noise at a 3-MHz offset is -140 dBc/Hz. If V_{DD}=1.5 V, the power consumption is only 6.8 mW. This VCO also satisfies the GSM phase noise specifications at

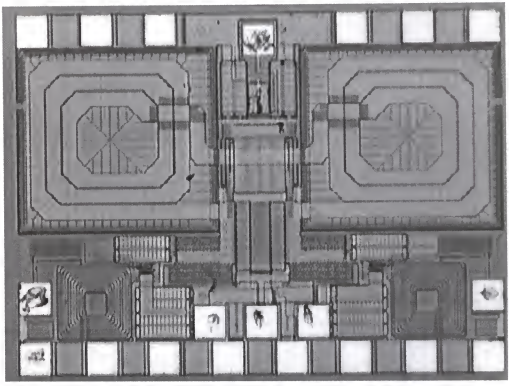


Figure 4-5 A die photograph of the VCO. The die size is 1.2x0.9 mm^2. A significant portion of the die is occupied by the inductors.

both 600-kHz and 3-MHz offsets of less than -121 dBc/Hz [52] and -135 dBc/Hz. Similar to the one in the previous section, this VCO is fabricated in a low cost 5-Volt, 0.8-μm foundry CMOS process with three metal layers, and is mounted in an SOIC like test package. The circuit topology (Figure 4-1) is the same as the previous VCO and exclusively uses buried channel PMOS transistors for lower 1/f noise.

4.3.1 Design Considerations

Figure 4-6 shows a bonding diagram for the chip and associated parasitic inductances. The two leads are connected in series with an external inter-

connect. As seen in Figure 4-6, this interconnect does not increase the board space beyond the area requirement for additional leads. Once again, inductor was optimized using Q factors estimated with the half-band-width method [16], [48]. The inductances of L1 and L2 were chosen to be ~7.1 nH. A concern for using this type of inductor is the inductance variation due to the variability of the bondwire length and the position of shorting wires relative to the leads, which could result in mismatches between L1 and L2, and could de-tune the center frequency ω_0. To reduce this effect, the PGS inductor was

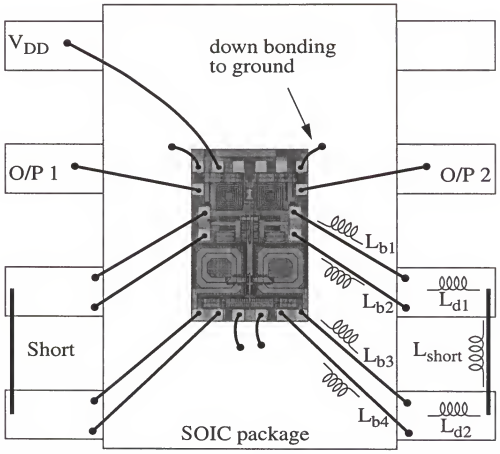


Figure 4-6 A bonding diagram for packaging the VCO. The inductor for the LC-tank utilizes a series combination of a short, 2 leads, 4 bondwires and an on-chip spiral inductor. The parasitic series resistances and shunt capacitances are not shown in the model.

designed to have an inductance of 2.15 nH which is ~28% of the 7.1-nH total inductance and double bondwires are used for each path between the lead and bonding pads to reduce the variable bondwire contribution to the total inductance.

Taking the self and mutual inductances of bondwires (L_{b1}-L_{b4}) and leads (L_{d1}-L_{d2}) (Figure 4-6) into account, and neglecting the mutual inductances between bondwires and leads, the total lead inductance $L_{d,tot}$ and total bondwire inductance $L_{b,tot}$ can be approximated as

$$L_{d,tot} = L_{d1} + L_{d2} - L_{m,(d1,d2)} \tag{4.1}$$

$$L_{b,tot} = \frac{L_{b1} \cdot L_{b2}}{L_{b1} + L_{b2}} + \frac{L_{b3} \cdot L_{b4}}{L_{b3} + L_{b4}} + L_M \tag{4.2}$$

$$L_M = L_{m,(b1,b2)} + L_{m,(b3,b4)} - L_{m,(b1,b3)} - L_{m,(b1,b4)} - L_{m,(b2,b3)} - L_{m,(b2,b4)} \tag{4.3}$$

where $L_{m,(a,b)}$ is the mutual inductance between L_a and L_b. The total inductance=$L_{b,tot}$+$L_{d,tot}$+L_{short}+L_{spiral}. The computed $L_{b,tot}$ and $L_{d,tot}$ are 1 and 2.71 nH, respectively. Assuming that the mutual inductances between the short and bondwires are negligible, the short contributes ~1.2 nH to the total. For the 2-nH PGS inductors, it was determined that the highest Q can be achieved when shunted metal 2 and 3 layers are used for the inductor trace. The area of the inductor is 300x300 μm^2. The metal spacing and width, and number of turns are 2 μm, 36 μm, and 2.25, respectively. The estimated parasitic capacitance seen looking into the PGS inductor is 0.95 pF. Through a sim-

ulation study, it was determined that the maximum mismatch between L1 and L2 while avoiding the second resonance [57] is ~1.71 nH (24%). Assuming 20% variation (which is very large) for the position of the shorting wires and the bondwire inductance, the maximum total inductance mismatch is 1.36 nH (19%) which is still low enough to avoid the problem. In an attempt to examine the variability, three VCOs were packaged manually and their tuned frequency at V_{DD}=2.7 V and power consumption of 12.7 mW has been measured. The tuned frequency ranged between 1.087 and 1.097 GHz which is only ~1% variation. If the VCOs are packaged using an automated equipment, the variability should have been even smaller. Because of the limited number of samples, it is not possible to conclusively claim that the variation is not a problem. At the same time, a large variability is not observed. The Q of the total inductor including the on-chip inductor, leads, bondwires and short connection, was estimated to be ~17 at 1.1 GHz (without taking the substrate effects into account). This in a combination with the lower 1/f noise of the buried channel PMOS transistors has led to the low measured phase noise at low power.

Since Q of the inductor is higher than that in the previous VCO, g_m of the cross-coupled transistors, M1 and M2, was chosen to be smaller (~8.4 mS at V_{DD}=2.7 V) than the previous. The 8.4 mS is ~4 times higher than that required for critical oscillation, which increases the signal level as well as the signal-to-noise ratio at the output. Using the layout optimization for M1 and M2 discussed in section 3.4, Q of ~57 at 1.1 GHz for C_{db} has been achieved. To obtain an oscillation frequency of 1.1 GHz with the 7.1-nH inductance and

0.95-pF parasitic capacitance, the sum of the varactor capacitance and transistor parasitic capacitances should be ~2 pF. The input capacitance of M1 and M2 (C_{gs}+C_{gd}+C_{db}) is ~0.9 pF, while that of the buffer transistor is ~0.2 pF. These leave ~0.9 pF for the varactor. The varactor is implemented in the same way as that for the previous VCO and has a Q of ~24 at 1.1 GHz and 0-V bias.

4.3.2 Experimental Results and Discussions

The measurement system has a noise floor of -102 dBm for a 10-kHz resolution band width (RBW). If the output power from the VCO is -17 dBm, then the 600-kHz offset phase noise of -126 dBc/Hz is very close to the noise floor and the power measurement of the sideband is not very reliable. To improve the measurement accuracy, an external amplifier is connected at the output of the VCO. The amplifier has a gain of 42 dB, a noise figure of ~0.8 dB and a P_{1dB} of +26 dBm. The noise floor of the measurement system with the amplifier is increased to -97 dBm for the same RBW due to the noise contributed from the external amplifier. The dynamic range is improved by ~12 dB. Figure 4-7 shows a single-ended output spectrum with a 200-kHz span and a resolution bandwidth of 1 kHz. V_{DD}, $V_{control}$ for the varactor, and the current for the VCO core are 2.7 V, 2.7 V and 4.7 mA, respectively. The signal power at the 1.09 GHz is +25.34 dBm and the phase noise at 10 and 100-kHz offsets are -92 and -112 dBc/Hz, respectively. These are the lowest phase noise reported using a CMOS technology at 1 GHz when published. A phase noise plot up to the 600-kHz offset is shown in Figure 4-8 (symbol 'o'). The phase noise is -126

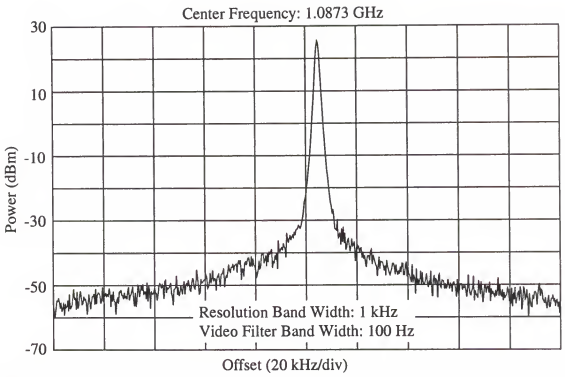


Figure 4-7 A 200-kHz span output spectrum (I_{vco}=4.7 mA, V_{DD}=2.7 V, and $V_{control}$=2.7 V). The power at the 1.09 GHz center frequency is +25.34 dBm. The phase noise at 10-kHz and 100-kHz offsets are -92 and -112 dBc/Hz.

dBc/Hz at a 600-kHz offset and is -140 dBc/Hz if extrapolated to a 3-MHz offset assuming a slope of -20 dB/dec. These easily exceed the GSM requirements of less than -121 [52] and -135 dBc/Hz at 600-kHz and 3-MHz offsets.

Oscillation frequency versus control voltage plots are shown in Figure 4-9. When the control voltage is decreased, the oscillation frequency is decreased. The tuning range shown in Figure 4-9 (symbol 'o') is ~103.7 MHz for the control voltage between 1.085 and 3 V and is 125.7 MHz if the control voltage is extended to 5 V. Over these frequency ranges, the GSM phase noise requirement is satisfied. For the control voltages lower than 1.085 V, the VCO still oscillates but the phase noise is too high to be used for GSM applications.

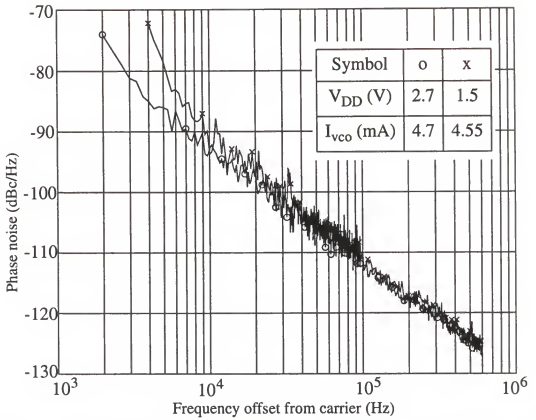


Figure 4-8 The phase noise at 10-kHz and 600-kHz offsets are -92 and -126 dBc/Hz, respectively when V_{DD}=2.7 V and I_{vco}=4.7 mA (symbol 'o'), and -90 and -125 dBc/Hz, respectively at V_{DD}=1.5 V and I_{vco}=4.55 mA (symbol 'x'). These exceed the GSM requirements of less than -121 [1] and -135 dBc/Hz, respectively.

As the oscillation frequency is lowered, Q of the LC tank is decreased. This reduces the signal level in the VCO core and increases the phase noise. More specifically, when the control voltage is lowered below 0.9 V, the dc voltage across the tuning diode becomes greater than +0.45 V, and the junction capacitance and average current flowing through the tuning diode both increase rapidly. These decrease Q of the tuning diode and thus, the internal signal level leading to an increase of the phase noise measured relative to the carrier power. Nevertheless, this VCO could be used in an up-side LO injected GSM

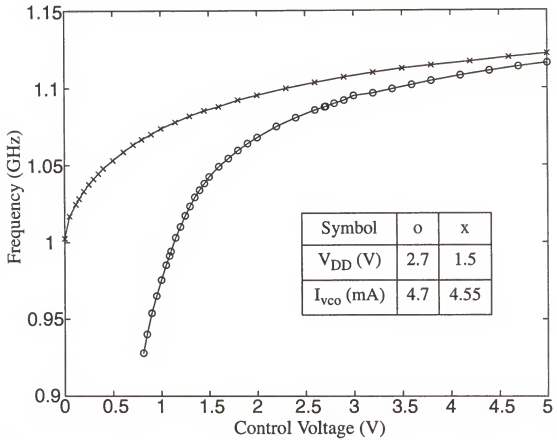


Figure 4-9 Oscillation frequency versus control voltage plots. The tuning range at V_{DD}=2.7 V and I_{vco}=4.7 mA (symbol 'o') is 103.7 MHz for the control voltage between 1.1 and 3 V and is 125.7 MHz if the control voltage range is extended to 5 V. At V_{DD}=1.5 V and I_{vco}=4.55 mA (symbol 'x'), the tuning range is 61.6 MHz for the control voltage between 0.12 and 1.5 V and are 83.4 and 97.4 MHz if the voltage range is extended to 3 and 5 V, respectively. Over these frequency ranges, the GSM phase noise requirements are satisfied. At control voltages below the mentioned lower limits, the VCO still oscillates but the phase noise is too high for GSM applications.

system with an IF frequency of 70 MHz. Increasing the current for the VCO core above 4.7 mA does not significantly reduce the phase noise since the internal voltage swing is near its maximum. However, the tuning range limited by the phase noise specification can be increased at the low frequency side

due to a larger g_m which increases the internal voltage swing and hence the signal-to-noise ratio at these frequencies.

The VCO core also works at 1.5-V V_{DD}. The phase noise plot is also shown in Figure 4-8 (symbol 'x'). When the control voltage is 1.5 V, the center frequency is 1.09 GHz. The bias current for the VCO core is 4.55 mA which corresponds to a power consumption of ~6.8 mW. The phase noise at a 600-kHz offset is -125 dBc/Hz and is -139 dBc/Hz if extrapolated to a 3-MHz offset. The tuning range is 61.6 MHz for the control voltages between 0.12 and 1.5 V and is 83.4 and 97.4 MHz if the control voltage range is extended to 3 and 5 V, respectively (Figure 4-9, symbol 'x'). The phase noise requirement of -135 dBc/Hz at a 3-MHz offset is satisfied within these tuning ranges. At 1.5-V V_{DD}, due to a lower dc voltage at the drains of M1 and M2, the capacitance of the tuning diode at the same control voltage is smaller than that when V_{DD} is 2.7 V. This results in a higher oscillation frequency at a given control voltage. At this supply voltage, once again, increasing the tail current does not significantly improve the phase noise because the internal voltage swing is at its maximum.

Figure 4-10 is a die photograph of the VCO. The die size is 1.2x0.8 mm^2. A significant portion of the die is still occupied by the spiral inductors. All bond pads once again have a polysilicon ground shield underneath to reduce the substrate coupling. Empty space in the circuit layout is once again filled in with p^+-substrate contacts to reduce the substrate coupling while not forming any closed loops around the inductors.

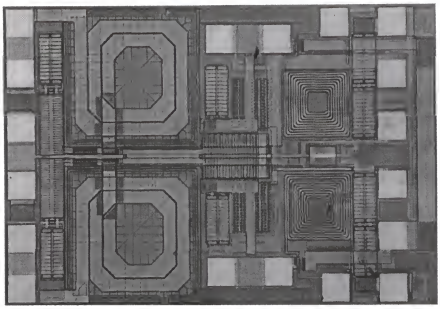


Figure 4-10 A die photograph of the VCO. The die size is 1.2x0.8 mm^2. A significant portion of the die is occupied by the inductors.

4.4 5-GHz LC-VCOs

5-GHz wireless applications such as High Performance Radio LAN (HIPERLAN) are gaining momentum. The requirements of a frequency synthesizer for such applications are low power, low cost, and low phase noise. For the VCO, the varactor Q degrades as the operating frequency is increased, while scaled MOS transistors required for 5-GHz operation have increased 1/f noise and a reduced supply voltage which decreases the voltage swing. All of these could make it difficult to achieve low phase noise at 5 GHz. In this section, three VCOs operating above 5 GHz are presented. The circuits have been implemented in a 0.25-μm CMOS process on p^- substrates (~8 Ω-cm) and 5 metal layers. With a high-resistivity substrate, the inductor Q can be

improved since the substrate effect [45] is smaller. The circuit topology is the same as the 1-GHz VCOs implemented in the 0.8-μm CMOS process. The inductors for the LC-tanks are implemented using an on-chip PGS spiral inductor for the first 2 VCO (referred as VCO-1 and VCO-2), and a series combination of a PGS inductor and a bondwire for the other (referred as VCO-3). A diode array structure is used in VCO-1 for frequency tuning while an MOS capacitor is used in VCO-2. Compared to the 1-GHz VCOs, the required current (I_{tail}) and G_m are lower because of the higher substrate resistivity and thus higher Q for the inductor. Due to the lower supply voltage (1.5 V) used in the VCOs, the power consumption is further reduced. Finally, the performance of fabricated VCOs on the p^- substrate is compared with those fabricated on p^+ substrates.

4.4.1 Transistor Noise

In the 0.25-μm CMOS process, both NMOS and PMOS transistors are surface channel devices, and a concern is that PMOS transistors may have the same poor 1/f noise performance as that of NMOS transistors. However, measurements [18] show that the PMOS 1/f noise is ~8-10 times smaller at 100 kHz for the same transistor dimension and gate over-drive ($V_{GT}=V_{GS}-V_T$) when the V_{GT} is smaller than ~0.3 V (used for the VCO core) [18]. Considering that a PMOS transistor has lower mobility, PMOS 1/f noise should be even lower at a given current and g_m due to a larger gate width and gate area (Eq. 2.11). In addition, the hot carrier effect in a PMOS transistor is smaller [20].

This is especially important in a deep submicron CMOS process where hot electron noise (white noise) is significant. Thus, utilization of only PMOS transistors in the VCO core should reduce the phase noise in the $1/f^3$ region (resulting from 1/f noise) as well as the noise in the $1/f^2$ region, which is mainly from the device white noise [9].

4.4.2 Design Considerations

The circuit topology used for the 5-GHz VCOs is the same as that in Figure 4-1. As mentioned in section 4.2.1, this circuit topology has reduced phase noise contributed from the bias circuit. However, given a constant gate voltage for the bottom transistor ($V_{g,m3}$), the quiescent bias point of the VCO core has a strong dependence on the power supply voltage. That is, the tail current and the dc voltages at drain nodes of M_1 and M_2 would change when the supply voltage varies. The AM and FM noise due to supply noise would therefore be significant and the phase noise performance would be degraded. To overcome this drawback, a replica bias circuit [58] is designed and integrated with the VCOs to control $V_{g,m3}$ in order to decrease the power supply dependence. Figure 4-11 shows a circuit schematic of the VCO with its bias circuit. As in the case of 1.1-GHz VCOs, cross-coupled transistors, M_1 and M_2, form a positive feedback loop to provide negative resistances to cancel the loss in the LC tanks. M_4, M_5, L_3 and L_4 form buffers capable of driving 50 Ω (spectrum analyzer). The bias circuitry consists of a current mirror (M_{N1} and M_{N2})

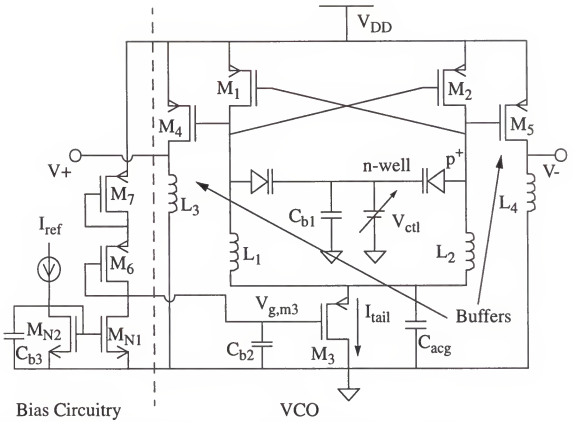


Figure 4-11 A circuit schematic of the 5-GHz VCOs with a replica bias circuit.

and two diode connected PMOS transistors (M_6 and M_7). The W/L ratios of M_6 and M_7 were scaled down by ~48 times from the equivalent half circuit of the VCO core to reduce power consumption of the bias circuit. Since M_7 replicates the bias condition of M_1, which is diode-connected at dc, the source voltages of M_3 and M_6 are the same. V_{gs} of M_6 which is kept constant by the current mirror at the bottom is replicated in M_3 to keep the bias current of the VCO constant. W/L ratios for both M_{N1} and M_{N2} were chosen to be reasonably large to increase the voltage range of $V_{g,m3}$ while keeping M_{N1} in saturation. To increase the output resistance of M_{N1}, a longer channel length MOSFET was

used. The channel length and width of both M_{N1} and M_{N2} are 1.74 and 96 μm, respectively. The power consumption of the bias circuitry is designed to be less than 4% of that of the VCO core. The drain node of M_{N2} is bypassed to ground using a 20-pF on-chip capacitor. Measurements show that the bias circuitry together with the utilization of a PMOS transistor at the bottom (4.2.1) has immeasurable impact on the overall phase noise performance.

4.4.3 Experimental Results of VCO-1

The LC tank of the VCO is formed using an inductor with a silicided polysilicon patterned-ground shield (PGS) [43], a p^+/n-well diode array (section 3.3.2), and the parasitic capacitances (C_{gb}, C_{gs} and C_{db}) of M_1 and M_2. The inductance was chosen to be large (~1 nH) for lower power consumption while maintaining a sufficient frequency tuning range. The measured inductor Q factors are shown in Figure 4-12. Q_{bw} [16] is 7 at 5.5 GHz (symbol '◇'). The quality factors of the other passive components, varactor and transistor capacitances present in the LC-network are also shown in Figure 4-12 and are 57 and 25 at 5.5 GHz, respectively when the bias voltages are 0 V (low-Q condition). Since the inductance and capacitance are small (~1 nH and ~140 fF, respectively), the layout and wiring between transistors, inductors and diode arrays must be reduced to minimize parasitic inductances and capacitances, which would degrade the overall Q of the tank and shift the resonant frequency.

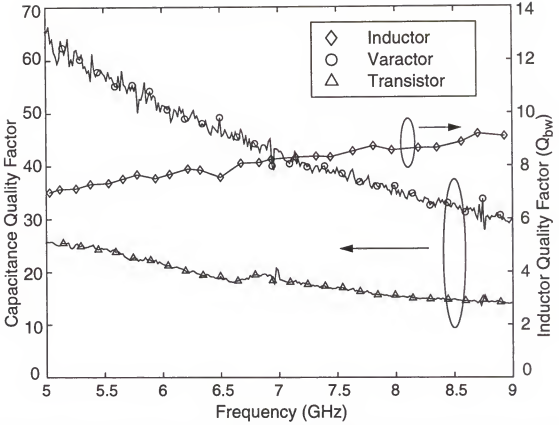


Figure 4-12 Quality factors of the passive components present in the LC tank of VCO-1. The bias conditions of the varactor and the transistor parasitic capacitances are 0 V.

A VCO output is connected to a spectrum analyzer through an external amplifier with a gain of 24 dB and a noise figure of 4.2 dB while the other output is terminated by a 50-Ω terminator. With 1.5-V V_{DD} and control voltage (V_{ctl}), and 4.7-mA tail current (I_{tail}), the measured carrier frequency is 5.35 GHz. The corresponding single side band (SSB) phase noise plot is shown in Figure 4-13. The phase noise at 100-kHz and 1-MHz offsets are -93 and -117 dBc/Hz, respectively. This VCO consumes less power and has phase noise which is more than 7 dB lower than those of the previously published 5-GHz CMOS VCOs [59], [60]. If the tail current and V_{DD} are increased to 6 mA and

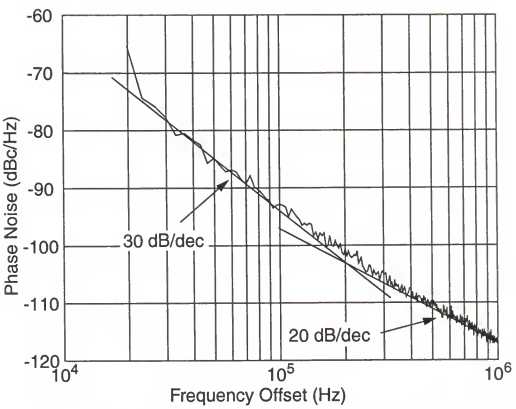


Figure 4-13 An SSB phase noise plot for VCO-1. V_{DD} and the tail current (I_{tail}) are 1.5 V and 4.7 mA, respectively.

2.5 V, the phase noise at the 1-MHz offset can be decreased to -119 dBc/Hz. An oscillation frequency versus V_{ctl} plot is shown in Figure 4-14. The tuning range is 336 MHz for V_{ctl} between 0.1 and 1.5 V. The phase noise is degraded by 3 dB at V_{ctl}=0.1 V. Since this 0.25-μm process is a 2.5-V process, the frequency at 2.5-V V_{ctl}, which is ~5.42 GHz was also measured. Thus, the tuning range becomes ~400 MHz. As will be discussed in the next chapter, a voltage doubler can be implemented on chip to generate ~2.5 V for charge pump to achieve a wider tuning range with 1.5-V supply voltage.

Shown in Figure 4-15 is a die photograph. The total area of the VCO including the pad frame is 581x470 μm^2. Similar to the 1-GHz VCOs, to

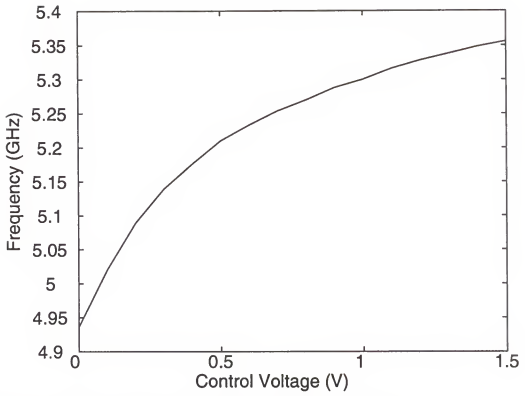


Figure 4-14 The frequency tuning characteristic of VCO-1.

reduce substrate coupling, all the bond pads have a polysilicon ground shield underneath, and empty areas are filled in with p-substrate contacts while not forming a closed loop around the inductors.

4.4.4 Experimental Results of VCO-2

This VCO is exactly the same as VCO-1 except the implementation of varactors. The primary purpose is to investigate the potential advantages and disadvantages using an MOS capacitor as a varactor. The MOS capacitor structure has an advantage of achieving a high quality factor. The series resistance originating from the nwell and polysilicon gate can be made smaller than the resistance from the metal interconnect [31], especially in a deep sub-

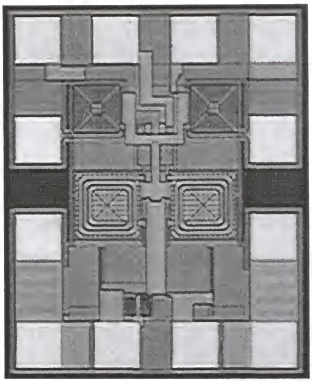


Figure 4-15 A die photo of VCO-1.

micron CMOS process where gate length and width can be made very small. In addition, the number of contacts and vias for both the top and bottom plates of a MOS varactor can be increased to reduce the overall resistance contribution from these contacts and vias. The ultimate limitation of Q for an MOS varactor in a deep submicron process is from the total series resistance of the metal interconnects, contacts and vias. On the other hand, the series resistance of the pn-junction varactor mainly originates from the n-well resistance between p^+ and n^+ diffusions. Because the minimum n-well width is much larger than the minimum gate length of an MOS varactor, the Q of the p^+/n-well varactor is lower than that of the MOS varactor. Thus, from the quality factor point of view, the MOS capacitor structure is superior. Another

advantage of the MOS varactor is that the maximum and minimum capacitances (in accumulation and depletion regions, respectively) can be reached within ~2 V of gate bias range (section 3.2.5). Therefore, an MOS varactor is naturally suitable for low voltage operation. Furthermore, because the bias voltage and thus capacitance range does not need to be limited like that for a p^+/n-well varactor to avoid turning on the diode, an MOS varactor potentially has a larger tuning range. Since the voltage dependence of the MOS varactor capacitance between depletion and accumulation regions is more linear than that of a p^+/n-well varactor, the frequency linearity of a VCO using MOS varactors should be better than that using p^+/n-well varactors. The frequency linearity is desirable in a phase-locked loop application to have a constant loop gain so that the frequency response and the stability of a PLL would not be varying over the entire frequency tuning range.

Although Q of an MOS varactor can be much higher than a pn-junction varactor Q, there are disadvantages associated with the capacitance characteristics. As discussed in section 3.2.5 and will be presented in section 4.6, the polysilicon depletion effect which potentially exists in deep submicron CMOS processes makes the VCO frequency tuning characteristic non-monotonic at high gate biases. Since a phase-locked loop (PLL) requires a VCO with a monotonic frequency tuning characteristic, the bias condition of a VCO using an MOS varactor must be carefully designed such that the polysilicon depletion effect is negligible, or a VCO should be designed such that the circuit will not operate in the regime where the polysilicon depletion effect is problematic.

For the latter case, considering the margin needed for the control voltage to overcome the process and temperature variations, the penalty on frequency tuning range could be significant.

The phase noise performance of this VCO using MOS varactors (VCO-2) is measured using the same setup as that for VCO-1. The SSB phase noise plot is shown in Figure 4-16 (symbol 'Δ') when V_{DD}=1.5 V, V_{ctl}=0.3 V and I_{tail} is 5 mA. The corresponding carrier frequency and phase noise are 5.23 GHz and -116.5 dBc/Hz at a 1-MHz offset, respectively. The phase noise plot for VCO-1 in Figure 4-13 is also shown in the same figure (symbol '☆') for comparison. The V_{ctl} of VCO-2 was chosen such that the MOS varactor is at its

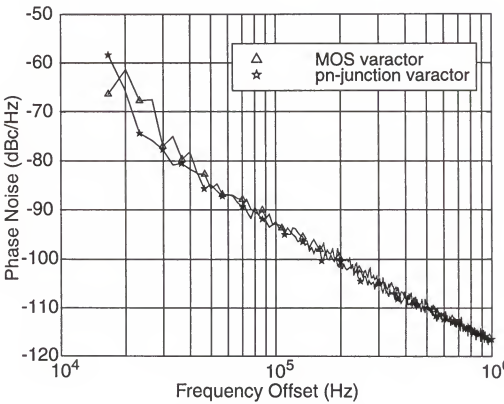


Figure 4-16 SSB phase noise plots for VCO-1 and VCO-2. V_{DD}, V_{ctl} and I_{tail} are 1.5 V, 0.3 V and 5 mA, respectively for VCO-2.

high-Q condition (Q is ~60). Since the quality factor of the varactors are much higher than the inductor Q (~7 at 5.5 GHz), as expected, the phase noise performance of VCO-2 is similar to that of the VCO-1. Q of ~60 for the MOS varactor is not the highest that can be achieved in this process. An MOS varactor with Q > 140 at 5.5 GHz has been measured using a varactor with a finger length and width of 0.24 and 0.6 μm, respectively. However, because the inductor Q is relatively low, increasing the varactor Q does not significantly improve the phase noise performance. Since Q of 57 for the pn-junction varactor at 5.5 GHz is more than adequate, the better Q of an MOS varactor is not a compelling reason for its use at 5.5 GHz. If the oscillation frequency were increased to much higher than 5.5 GHz, the inductor Q could be significantly higher. In this situation, the tank Q can be limited by the varactor Q, and it would be beneficial to use MOS varactors with higher Q for the LC-resonators. An oscillation frequency versus V_{ctl} plot is shown in Figure 4-17 (dashed line). The tuning characteristic of VCO-1 in Figure 4-14 is also shown in the same plot (solid line) for comparison. The tuning range is ~310 MHz for V_{ctl} between 0 and 1.5 V. Since Q of the MOS varactor is higher at low V_{ctl} (section 3.2.5), the phase noise is lower at 0-V V_{ctl} which is opposite to VCO-1. The phase noise is degraded by 1 dB at V_{ctl}=1.5 V. The phase noise flatness over the entire tuning range is another advantage of using an MOS varactor. As expected, the tuning characteristic (VCO gain) of VCO-2 is more linear than that of VCO-1 which would result in a smaller VCO gain variation. The smaller variation of VCO

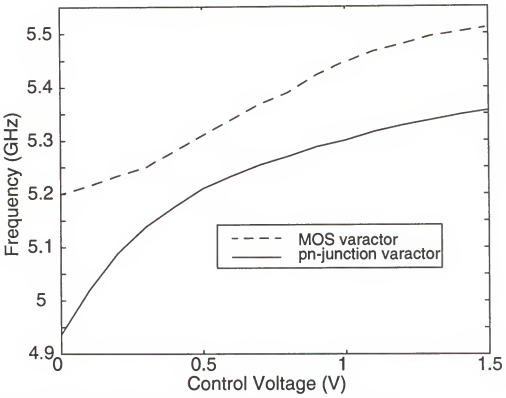


Figure 4-17 The frequency tuning characteristic of VCO-2.

gain could simplify a PLL design since a circuit for linearization of the VCO gain may be eliminated.

4.4.5 Experimental Results of VCO-3

The excellent performance of the 1.1-GHz VCO using package parasitics [56] motivated use of bondwire inductance in the LC tanks for a 5.5-GHz VCO. Since the total inductance needed for 5.5 GHz operation is ~1 nH, only a bondwire (instead of a combination of bondwires and package leads) is utilized in the inductor design in addition to the on-chip PGS spiral inductor. To reduce the variability, the targeted inductance distribution is 50% (0.5 nH) for both bondwire and spiral inductor. The length of a bondwire needed for 0.5-nH

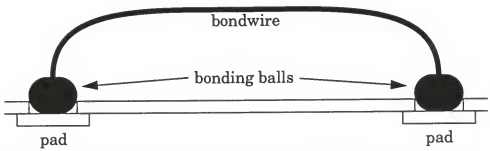


Figure 4-18 A cross-sectional view of the bondwire between two pads.

inductance is ~610 μm. Considering that the bondwire has ~60-μm height and is not straight between bonding pads (Figure 4-18), the distance of the pads should be ~490 μm. Figure 4-19 is a die photograph of VCO-3 and shows the configuration of bondwires. The two bondwires are in parallel and are separated by ~130 μm. The mutual inductance is estimated to be ~0.19 nH which means that the total inductance would become ~0.8 nH and the corresponding resonant frequency is ~1.1 ($1/\sqrt{0.8}$) times higher. Since the height of the bondwires is variable and could be higher when manually bonding, the distance is kept unchanged. To simulate the coupling between these two bondwires in Spice, the bond-wire inductors were modeled as a transformer. The coupling factor k is calculated by $\frac{M}{\sqrt{L \cdot L}} = \frac{M}{L}$ [14], where M and L are mutual and self inductances, respectively. Since MOS varactors are used for this VCO, the frequency tuning range is expected to be similar to VCO-2.

In the VCO layout, the metal lines for ground connection, two bypass capacitors and the gate capacitances (C_{gs} ~ 550 fF and C_{gd} ~ 130 fF) of M_3 form a closed loop surrounding the 0.5-nH PGS inductor. Since the channel width of M_3 is large (~490 μm), C_{gd} of M_3 and thus the effects of the closed

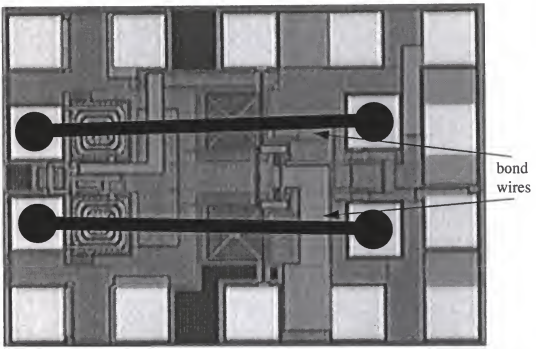


Figure 4-19 A die photo of the 6-GHz VCO using bondwires and PGS inductors (VCO-3).

loop at 5.5 GHz is not negligible. The closed loop decreases the inductance and Q of the 0.5-nH PGS inductor resulting in a higher oscillation frequency. The bondwires were attached using a ball bonder. Figure 4-20 shows a frequency tuning characteristic for the VCO. The tuning range is ~325 MHz for the control voltage between 0.1 and 1.5 V. Due to the Q degradation resulting from the bondwire configuration and the closed loop around the PGS inductors, the VCO needs a minimum current of ~7 mA to oscillate. An SSB phase noise plot is shown in Figure 4-21 when V_{DD}, V_{ctl} and I_{tail} are 1.8 V, 0.1 V and 9 mA, respectively. The phase noise is -117 dBc/Hz at a 1-MHz offset from the 5.16 GHz carrier.

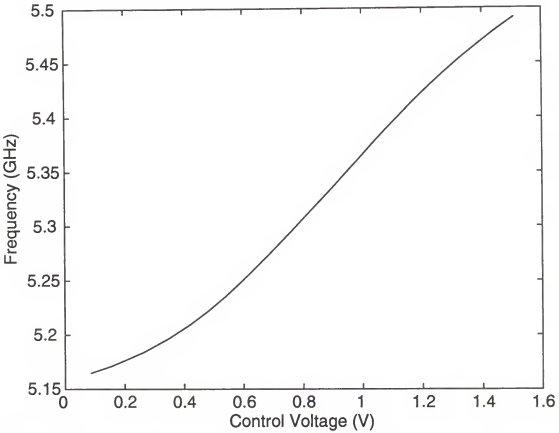


Figure 4-20 Frequency tuning range of VCO-3. The tuning range is ~300 MHz V_{DD} and I_{tail} are 1.5 V and 8.4 mA, respectively.

4.5 A 9-GHz Dual-Phase Relaxation VCO

A dual phase ring oscillator was designed using a Spice model for an experimental 0.1-μm CMOS process [61]. The VCO was then fabricated on a bulk substrate using the same masks. The process uses a partially scaled 0.35-μm design rule set except for the minimum polysilicon gate length of 0.1-μm. Hence, significant parasitics can be expected.

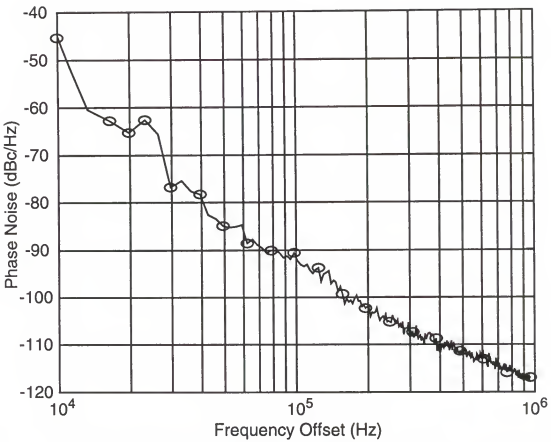


Figure 4-21 SSB phase noise plots for VCO-3. V_{DD}, V_{ctl} and I_{tail} are 1.5 V, 1 V and 8.4 mA, respectively for the 6.5-GHz version and are 2.1 V, 0 V and 9 mA, respectively for the 5.16-GHz version.

4.5.1 Design Considerations

Figure 4-22 shows a circuit schematic of the voltage-controlled ring oscillator including buffers. M1-M13 form a three-stage dual-phase ring oscillator. The oscillation frequency is controlled by varying the current and thus the delay time of the second stage. When the input voltage of M13 is increased, both channel current and the oscillation frequency increase. The outputs should be 180^0 out of phase due to the differential connection of the

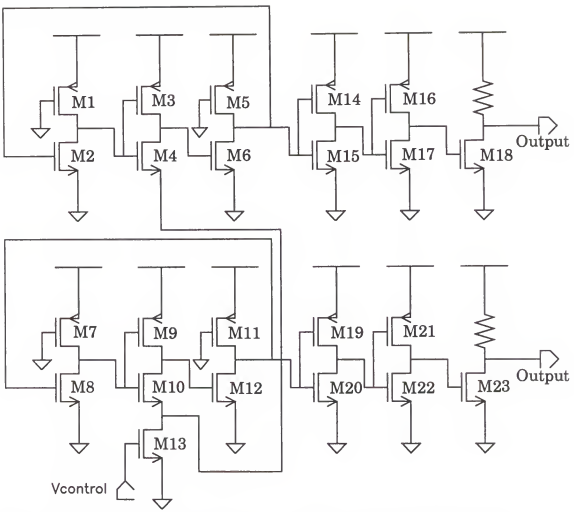


Figure 4-22 A circuit schematic of the 12-GHz VCO including buffers.

second stage. To increase the speed, a pseudo NMOS configuration is used for the first and the third stages, while the second stage uses a conventional inverter structure to maintain sufficient gain for oscillation. The current of the two pseudo-NMOS stages are not controlled so that they can operate at their highest speed. A disadvantage is that the tuning range becomes smaller since the variability of the oscillation period ($2\pi/\omega_0$) depends only on the propagation delay of the second stage. The buffer consists of two stages of CMOS inverters and one stage of common source amplifier. The first inverter in the

buffer is made small so that the input capacitance does not significantly load the third stage inverter in the VCO core. The width of the transistor in the common source amplifier was chosen to provide an adequate driving capability for a 50-Ω load.

4.5.2 Experimental Results

Due to the unavailability of the wafers, the characterization was not completed. Only the tuning range and power consumption data were measured. In addition, because of the exploratory nature of the process, the number of working VCOs is limited. Figure 4-23 shows a tuning range versus

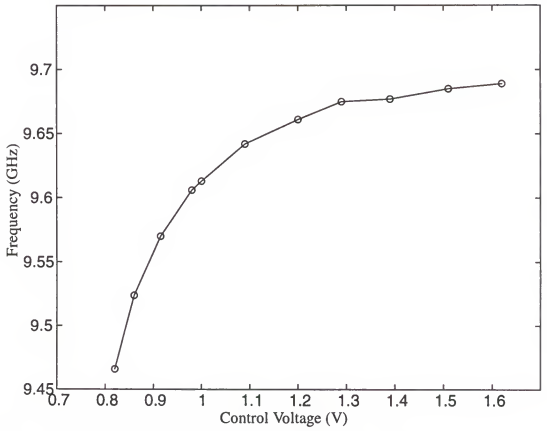


Figure 4-23 Oscillation frequency versus control voltage plots.

control voltage plot for the VCO on a bulk substrate. The oscillation frequency at V_{DD}=1.6 V ranges between 9.47 and 9.68 GHz corresponding to a tuning range of 230 MHz for the control voltage between 0.83 and 1.63 V. The current for the VCO core is ~23.5 mA and the power consumption is ~37.5 mW. The phase noise of the VCOs were not measured. This was measured in Spring 1997, and this was the bulk CMOS circuit with the highest operating frequency.

4.6 LC-VCOs at >20 GHz

4.6.1 Circuit Description

Figure 4-24 shows a circuit schematic of the 24-GHz VCO [62]. This is similar to the one in Figure 4-1 except that only NMOS transistors are used for higher g_m and smaller parasitic capacitances (i.e. higher f_t). L_1, L_2, C_{v1}, and C_{v2} form two LC resonant networks for the VCO. The cross-coupled NMOS transistors, M_1 and M_2, form a differential pair providing negative resistances to cancel the loss in the tanks sustaining the oscillation. The oscillation frequency is controlled by varying the capacitances of C_{v1} and C_{v2} which were implemented using high-Q MOS capacitors. The current of the VCO core is controlled by the gate bias of M_3. This configuration has a lower conversion gain from gate to source node of M_3, which reduces the phase noise contribution from a bias circuitry connected to V_g (section 4.2.1). The bias circuit of this VCO can be designed using a similar circuit schematic discussed in section 4.4.2. To reduce the voltage ripple at source of M_3 ($V_{s,m3}$) which would

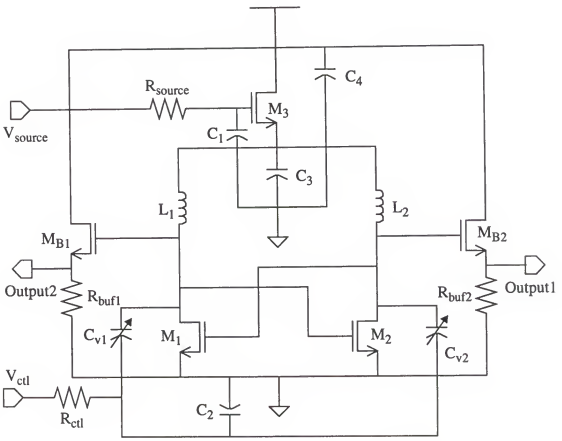


Figure 4-24 A circuit schematic for the 24-GHz VCO.

modulate the bias of the VCO core resulting in phase noise degradation, a high-Q MOS capacitor [31] C_3 is connected between $V_{s,m3}$ and ground. Capacitors C_1, C_2, and C_4 are for bypassing the power and ground line inductances. Q of these three capacitors is chosen to be high (~20 @ 26 GHz) to properly bypass the power and ground line inductances. The buffer is a source follower and is designed to drive 50 Ω (input impedance of the spectrum analyzer). Resistors R_{buf1} and R_{buf2} will add noise. However, the offset frequency of interest is usually sufficiently close to the carrier (less than a few MHz) that the VCO noise amplitude is far greater than the buffer noise floor [63].

4.6.2 Experimental Results and Discussions

This VCO has been fabricated in an IBM 0.1-μm (L_{eff}) bulk CMOS process. There are 2 layers of metal available and the substrate resistivity is ~1-Ω-cm. The process uses a 0.35-μm design rule set except for the L_{eff}. The gate oxide thickness is 3 nm and the threshold voltage is ~0.3 V. The inductors are implemented using a 1.75-turn spiral inductor. Shunted metal 1 and 2 layers are used for the inductor trace. The measured composite metal sheet resistance is ~40 mΩ/□. The inductance is designed to be ~0.2 nH. The metal width and turn spacing are 8 and 1 μm, respectively. The inductor area is ~2000 μm^2. Since only two metal layers are available, the inductor series resistance and parasitic capacitance are high. Additionally, the high operating frequency and relatively low substrate resistivity further degraded inductor characteristics. The varactor is realized using a high-Q MOS varactor [31], [64] shown in Figure 4-25. The top plate formed by 0.1-μm long polysilicon gate (8 Ω/□) is connected to the tank while the bottom plate formed by n-well (500 Ω/□) and n^+ diffusion is tied together, and bypassed to ground using another 20-pF MOS capacitor (C_2). The VCO frequency is tuned by changing the bottom plate (n-well) bias. A measured capacitance plot versus the voltage across the top and bottom plates of the varactor is shown in Figure 4-25. For dc voltages greater than 0.4 V, capacitance decreases with the bias. This is due to the polysilicon gate depletion effect [39], which also decreases the maximum capacitance (C_{max}). As the polysilicon gate length is reduced (Figure 4-25) to

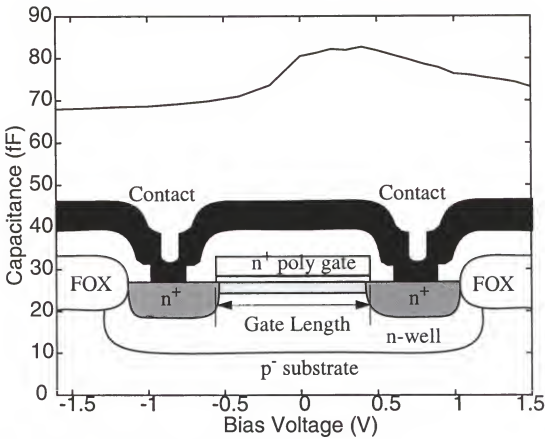


Figure 4-25 A C-V plot (L_{eff} = 0.1 μm) and a cross section of the varactor.

increase Q of the varactor (section 3.2.1), the overlap and fringing capacitances contribute more to the total capacitance. This decreases the ratio between C_{max} and minimum capacitance. Q versus frequency plots at the highest and lowest Q conditions for the bias range used in the VCO are shown in Figure 4-26. The highest and lowest Q factors are ~40 and ~20 at 26 GHz, at the top-to-bottom plate voltages of -1 and 0.4 V, respectively. These are excellent results considering that the varactor Q is inversely proportional to frequency and the bottom plate of the structure is formed with the high-sheet-resistance n-well layer. Despite this, Q of the varactor is a factor limiting the tank Q at such a high frequency.

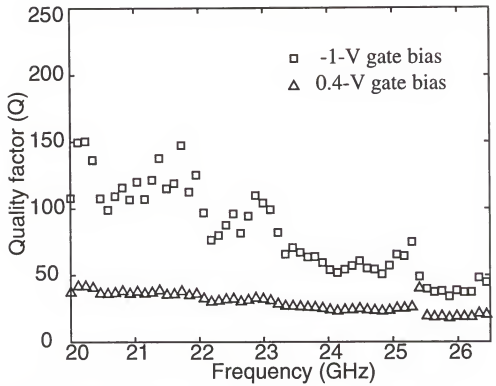


Figure 4-26 Q versus frequency plots for gate biases of 0.4 and -1 V.

The bias condition of the VCO is determined by the gate voltage of M_3 ($V_{g,m3}$). If $V_{g,m3}$ is increased, the current flowing into the VCO core and the voltage at drain node of M_1 (M_2) would be increased. The resulting power consumption is higher and the VCO oscillation frequency is lower for a given control voltage (V_{ctl}) since the bias voltage across the varactor is smaller. The bias condition was chosen such that the VCO has good phase noise performance within the whole frequency tuning range. That is, $V_{g,m3}$ was chosen to have enough current in the VCO core to overcome the loss when the varactor is at its low-Q condition. Figure 4-27 shows a VCO spectrum measured at one of the outputs across a 20-MHz span. The power level at the center frequency is -22 dBm and the spectrum is clean over the frequency span. The oscillation

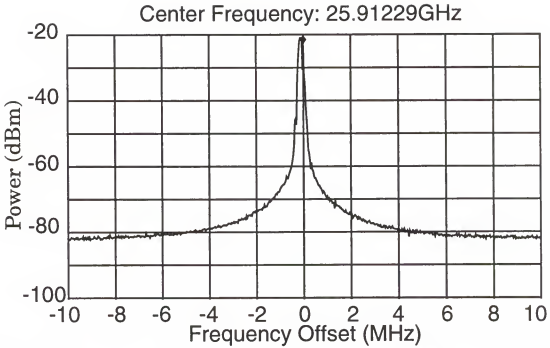


Figure 4-27 An output spectrum of the VCO across a 20-MHz span. The resolution bandwidth and video bandwidth are 100 kHz and 300 Hz, respectively.

frequency of 25.9 GHz is higher than the simulated (24 GHz) because the capacitances of C_{v1} and C_{v2} are smaller than those from simulations. The power consumption is ~24 mW from a 1.5-V supply for the VCO core while the buffers consume ~4.5 mW. A single-side-band (SSB) phase noise plot is shown in Figure 4-28. The phase noise is -106 dBc/Hz at a 3-MHz offset from the 25.9 GHz carrier. This VCO suffers from higher 1/f noise due to the small gate length and area as well as higher thermal noise due to larger hot electron effect than the 1-GHz PMOS VCOs. These with the lower varactor Q and higher inductor series resistance has led to the relatively high phase noise.

A frequency versus tuning voltage (F-V) plot is shown in Figure 4-29. The frequency tuning range is ~600 MHz for the control voltages (V_{ctl}) or the

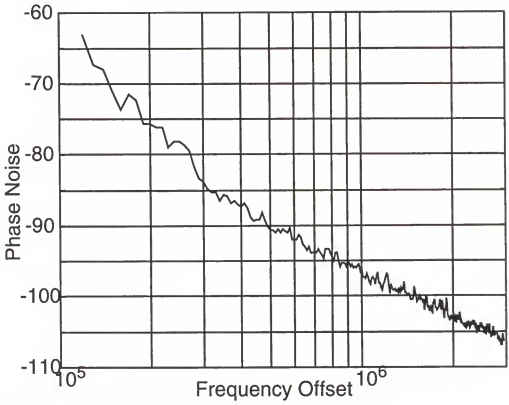


Figure 4-28 An SSB phase noise plot up to a 3-MHz offset.

varactor bottom plate voltages between 0.7 and 1.5-V. The top plate voltage of the varactor is ~1.1 V. When V_{ctl} is less than 0.7 V, the oscillation frequency decreases with the control voltage. This is due to the polysilicon depletion effect which decreases the capacitance when the voltage across the varactor is higher than 0.4 V. This is potentially problematic when the VCO is used in a phase-locked loop (PLL). If the VCO is operated in the undesired region, the PLL may never be able to lock since the F-V characteristic in region 1 is the opposite of that in region 2 (Figure 4-29). A mechanism to limit the voltage range of V_{ctl} is needed. The phase noise and output power level flatness across the 1.5-V control voltage range are less than 1 and 1.5 dB, which are excellent owing to the utilization of MOS varactors. The die photograph is shown in Fig-

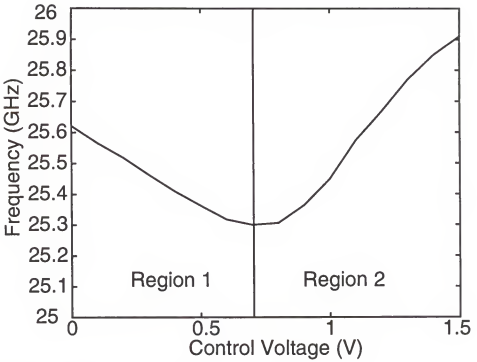


Figure 4-29 A frequency versus control voltage plot.

ure 4-30. The die size is 511x486 mm^2. All bond pads have a p^+-diffusion ground shield underneath to reduce substrate coupling.

4.7 The Effects of Substrate Resistivity on LC-VCOs

As demonstrated in section 3.5, the substrate resistivity has large effects on inductors which in turn significantly affects the performance of RF circuits. For LC-VCOs, as discussed before, the overall Q of the LC tank is the major limiting factor of the phase noise performance, where the tank consists of an inductor, a varactor, the gate and drain capacitances of M_1 and M_2, and the gate capacitance of M_4 and M_5 (Figure 4-11). The VCO is implemented in a 0.25-μm CMOS process with five metal layers on both p^+ (0.01-Ω-cm) with an

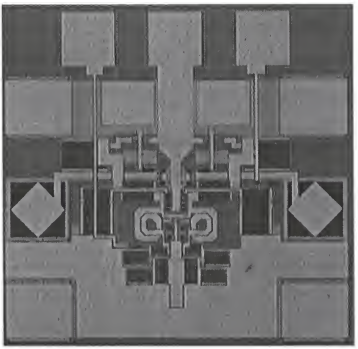


Figure 4-30 A die photograph of the 25.9-GHz VCO.

epitaxial layer and p^- (~8-Ω–cm) substrates. The measured Q of the 1-nH inductor (L_1 and L_2) is ~8.5 times smaller than that of the p^+-to-n-well varactor indicating that Q of the overall LC tank is limited by the inductor. Figure 4-31 shows the measured phase noise for the VCO on both p^+ and p^- substrates when the currents of the VCO core are the same. V_{DD}, V_{ctl} and I_{tail} are 1.5 V, 1.5 V and 4.7 mA, respectively. The carrier frequency is 5.35 GHz. Assuming that the tank resistance is dominated by the inductor resistance (tank Q ~ inductor Q), the phase noise of a VCO in the $1/f^2$ region can be approximated by

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log\left\{\frac{2FkT}{I^2 Q_{ind}^{\ 2} r_s} \cdot \left[1 + \left(\frac{\omega_0}{2Q_{ind} \cdot \Delta\omega}\right)^2\right]\right\} \qquad (4.4)$$

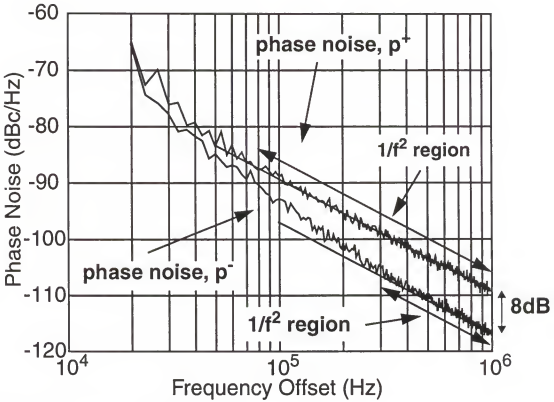


Figure 4-31 Measured VCO phase noise for p^- and p^+ substrates

where F is the noise factor of the amplifier, k is the Boltzmann's constant, T is the temperature, I is the root-mean-square (RMS) current supplied to the tank, Q_{ind} is the inductor Q, r_s is the series resistance of the inductor, ω_0 is the resonant frequency, and $\Delta\omega$ is the frequency offset from the carrier [9]. Assuming that the last term in the equation is much greater than 1, and all other parameters except r_s and Q_{ind} in the equation are constant, a 29% Q degradation (section 3.5) from 7 (p^- substrate) to 5 (p^+ substrate) increases the phase noise by ~7.3 dB (10 log$(7/5)^5$), which is a large difference. The measured difference in the $1/f^2$ region (straight lines in Figure 4-31) is ~8 dB which agrees well with the analytical prediction.

4.8 Summary

1.1 and 1.24-GHz VCOs implemented in a low-cost 0.8-μm foundry CMOS process have been demonstrated with superior phase noise performance than the previously reported 1-GHz VCOs. The VCOs satisfy the stringent GSM phase noise requirements. In addition, the tuning range is also adequate for GSM system. The power consumption of the former VCO is comparable to those fabricated in Si-bipolar processes [53], [65] while the latter consumes more power due to the induction loss in the p^+ substrate and the improper optimization of the inductors used in the LC-tank. These prototypes not only demonstrate the feasibility of RF VCO using CMOS technology but also facilitate the understandings of how to implement low-power and low-phase-noise VCOs. With these results as the foundation, VCOs and a PLL frequency synthesizer operating at ~5.5 GHz were designed and fabricated using a digital 0.25-μm CMOS process. Two 5.35-GHz VCOs using on-chip spiral inductors, and MOS and pn-junction varactors, respectively were implemented. These have the lowest phase noise reported to date for integrated VCOs at 5 GHz. A VCO using a combination of a bondwire and a spiral inductor was also implemented. However, due to a closed loop consisting of metal lines and capacitors around the spiral inductors, the phase noise performance and power consumption are worse than those of the integrated VCOs. The VCO using an on-chip spiral inductor and a pn-junction varactor for the LC-tank was also fabricated on a p^+ substrate. Due to a Q degradation for the

inductors on the p^+ substrate, the phase noise of the VCO on a p^- substrate is ~8 dB better (lower) than that on the epi wafer.

In addition to the 1 and 5-GHz frequency ranges, a VCO designed for >20 GHz as well as a VCO based on a ring of inverters were investigated. The measured data showed that voltage-controlled oscillators in CMOS processes operating above 30 GHz should be possible. These VCOs provided an early look on the possibilities of RF circuits operating at frequencies beyond 30 GHz using advanced CMOS processes.

CHAPTER 5
A 5.5-GHz CMOS FREQUENCY SYNTHESIZER

5.1 Introduction

Efforts on development of CMOS RF front end circuits have shown promising results for applications in 900-MHz and 1.8-GHz frequency bands. With the advances of CMOS processes, it has become possible for CMOS circuits to operate at higher frequency band such as 5-GHz band which has been allocated for wireless local area network (WLAN) and other ISM applications. This chapter describes the design and experimental results of a low-voltage low-phase-noise integrated frequency synthesizer operating at 5 GHz using a 0.25-μm digital CMOS process. The synthesizer includes a voltage-controlled oscillator (VCO), a divide-by-128 frequency divider, a phase/frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage doubler and level shift circuits. The supply voltage for the VCO and frequency divider is 1.8 V while that for the rest is 1.5 V.

As demonstrated in CHAPTER 4, VCOs operating at 1.5-V supply voltage and the 5-GHz frequency band with excellent phase noise performance are feasible. The other challenging circuit block in a frequency synthesizer which operates at RF is the frequency divider. The frequency divider must operate on low power and should have low switching noise, and are presented in sec-

tion 5.2. All the other circuit blocks needed to complete the frequency synthesizer including a PFD, a CP and an LF are presented in section 5.2. A voltage doubler is also designed and inserted into the phase-locked loop (PLL) to increase the voltage range of the VCO control input, thus increasing the tuning range of the VCO/frequency synthesizer. Finally, the layout considerations for integrating the PLL frequency synthesizer are briefly discussed in section 5.4.

5.2 Circuit Blocks of the 5.5-GHz Frequency Synthesizer

5.2.1 Divide-by-128 Frequency Divider

For a typical single-phase dynamic divider, the glitches and current pulses due to switching can inject a large amount of current into the substrate. Because the frequency divider is typically near the VCO, the divider noise can degrade the phase noise performance of the VCO. Thus, flip-flops with a differential structure [66] are used. In addition, the divider is designed to have low power consumption while capable of operating at high speed and low voltage.

The divide-by-128 prescaler is designed using 7 cascaded divide-by-2 circuits [67] shown in Figure 5-1 followed by a 3-stage inverter chain for driving a 50-Ω measurement system. To reduce the switching noise, a source-coupled logic (SCL) structure [66] is used and the voltage swing is kept as small as possible to avoid hard switching of M_1 and M_2 except for the first stage whose inputs are the VCO outputs which typically have a larger amplitude for

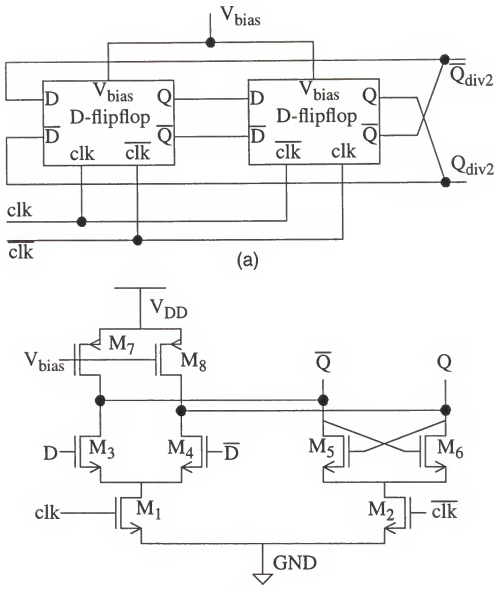


Figure 5-1 (a): A block diagram of the divide-by-2 circuit. (b): A circuit schematic of the D-flipflop.

lower phase noise. The small voltage swing also helps to increase the maximum speed since the time needed to switch from high (low) to low (high) is shorter. One of the key parameters being monitored and optimized during simulation is the current ripple at the V_{DD} node which is an indication of switching noise. Especially for the first stage whose input signal has a large

voltage amplitude and is at the highest frequency, its current ripple is potentially the largest in the whole divider. The simulated the peak-to-peak current ripple, I_{pp}, for the first stage is only 40 μA when the average current is 1.12 mA. This I_{pp} is very small compared to a conventional dynamic divider. The current source between the sources of M_1 and M_2 and ground in conventional SCL designs is omitted for low voltage operation. V_{bias} of the first 2 stages are grounded to increase the maximum operating frequency by operating M_7 and M_8 in the linear region. The resistances looking up from Q and $\overline{Q}$ are reduced while the capacitances are increased. Since in a deep submicron CMOS process, the overlap and fringing capacitances contribute more significantly to the total gate capacitance, the % increase of capacitance (%c) by changing the bias condition from saturation to linear regions is smaller. %c is also relatively smaller than the % decrease of resistance (%r). Hence, the overall RC time constant at $Q/\overline{Q}$ is reduced and the maximum speed is improved. Furthermore, when the output voltage of Q is increased (during a low to high transition), the resistance looking up from Q is decreased since v_{ds} and the output resistance of M_8 (in linear region) are decreased. This nonlinearity of M_8 helps to pull up Q to its logic high which in turn helps to increase the maximum operating frequency at a given power consumption level. Similarly, when Q is decreasing, the nonlinearity tends to push down Q to its logic low. In addition to the advantage of high speed operation, this topology has reduced power consumption compared to the topology in [54] due to the elimination of the folded diode-connected transistor from Q ($\overline{Q}$) to ground. The transistor sizes were

chosen such that the dc level and small-signal swing at the output of each stage can directly drive the subsequent stage without fully restoring the signal level. This further reduces power consumption and lowers switching noise. To decrease the switching noise coupling to an integrated VCO, large-area substrate contacts are used to isolate the circuit blocks from each other.

The divide-by-2 circuit may be thought as an injection locked oscillator [60]. When both clock transistors (M_1 and M_2) are turned on, the divide-by-2 circuit oscillates at a half of the frequency of the input signal (clk, $\overline{\text{clk}}$) [68]. If the input signal level is smaller than the required for injection locking to occur or the frequency of the input signal is outside the locking range, the divide-by-2 circuit self-oscillates at a frequency determined by the delay time of the flipflop. The delay time and thus the self-oscillation frequency varies with both the bias condition and the transistor sizes. When the input frequency is away from (both above and below) twice the self-oscillation frequency, the required input power is larger. The sensitivity is maximized at a frequency twice the self-oscillation frequency.

By increasing the sizes of M_1, M_2, M_7 and M_8 for the first 3 stages, the maximum operating frequency can be increased. The self-oscillation frequencies of the second and the third stages are also increased due to a reduced delay time of the flipflops. Since the output signal level of the first and the second stages are small and can not be arbitrarily increased, the minimum operating frequency (which is the lowest frequency in the locking range) of the divide-by-128 circuit is increased. The maximum speed of the divide-by-128

prescaler is determined by the first stage while the minimum operating frequency is determined mostly by the latter stages whose input signal levels are small. Fortunately, since the divider works for a frequency range over 77% of the maximum operating frequency which is much larger than the VCO tuning range, the limitation of minimum frequency is not an issue.

At 5.4 GHz, the prescaler, excluding the buffer formed by an inverter chain, consumes only 4.1 mW at 1.5-V V_{DD}. The power consumption of the first stage is ~1.65 mW which is comparable to that of an analog frequency divider [60], while the latter stages consume 1/5 of the power of the prescaler in [60]. The maximum operating frequency can be increased by increasing V_{DD} and current (Figure 5-2). As discussed earlier, when M_1, M_2, M_7 and M_8 in the first three stages (divide-by-8) are widened, the maximum operating

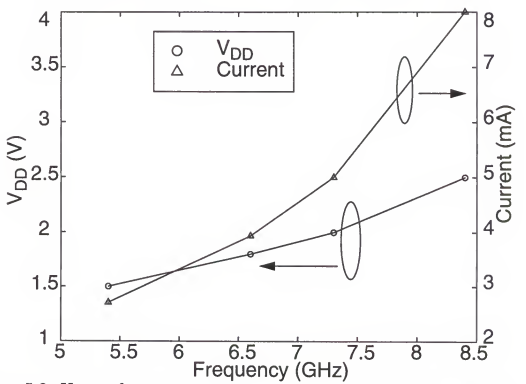


Figure 5-2 V_{DD} and current versus maximum operating frequency plots.

frequency can be increased. By widening these transistors by ~20%, a maximum operating frequency of 9.96 GHz is measured at 2.5-V V_{DD} and 7.36-mA total current for the first three stages [69]. The output waveform to a 50-Ω load for the second prescaler is shown in Figure 5-3. A 50-Ω measurement system is used to reduce the V_{DD} and ground bounce problem since the interest here is the phase instead of amplitude information.

To experimentally verify the low-noise performance, phase noise of a test circuit including a VCO (VCO-3 in CHAPTER 4) and the divide-by-128 circuit was measured. The VCO output is directly connected to the divider input as stated earlier. The divider was placed in the middle of the VCO for which the effects of the divider noise should be the severest. The VCO phase

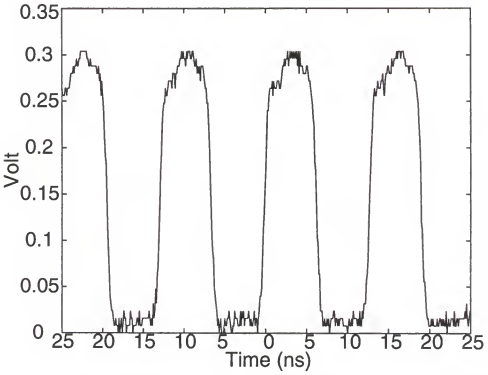


Figure 5-3 An output waveform of the prescaler with larger transistors in the first 3 stages at an input frequency of 9.96 GHz.

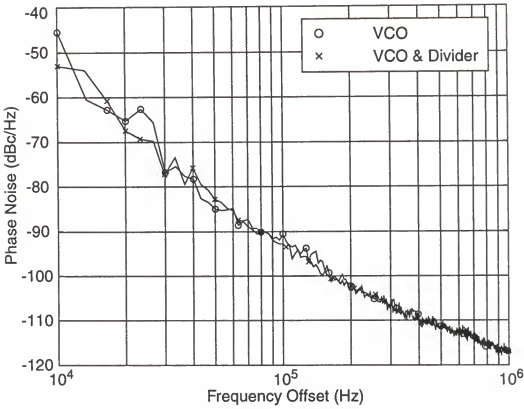


Figure 5-4 SSB phase noise plots for the VCO and divider combination. The phase noise is essentially the same indicating that the noise from the divider is low.

noise is measured when the divider was turned on and off, and is shown in Figure 5-4. The phase noise characteristics are essentially the same. The spurs at f_{div} (where $f_{div}=f_{vco}/128$ is the divider output frequency) in the VCO output spectrum is 74 dB below the carrier (Figure 5-5). Both substrate coupling and the coupling between metal interconnects and bondwires are responsible for the spurs. Nevertheless, these measurements indicate that the divider is quite. V_{DD}, V_{ctl} and I_{tail} are 1.8 V, 0 V and 9 mA, respectively. The oscillation frequency for this measurement is 5.16 GHz. The bias condition was chosen to be consistent with that used for the closed-loop frequency synthesizer measurement presented in section 5.3.

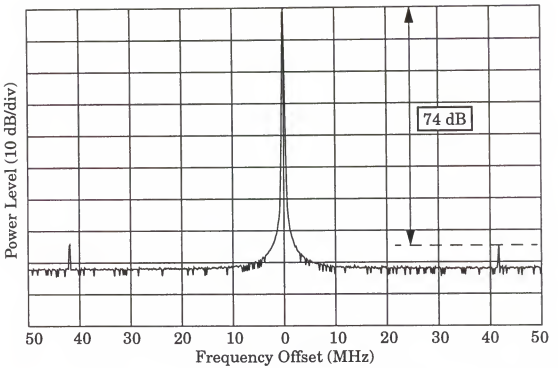


Figure 5-5 A VCO output spectrum when the frequency divider is turned on.

A die photograph of the prescaler is shown in Figure 5-6(a). The active area (excluding the pad frame) of the prescaler while including internal bypass capacitors is 181x244 μm^2. To reduce the substrate coupling, all the bond pads have a polysilicon ground shield underneath, and empty areas are filled in with p-substrate contacts. Figure 5-6(b) shows a die photograph of the VCO and divider combination. The divider is surrounded by p-substrate contacts to reduce the noise coupling.

5.2.2 Phase/Frequency Detector (PFD)

The phase/frequency detector compares the output signal (a pulse train) from the frequency divider (f_{div}) with an external reference source (f_{ref}).

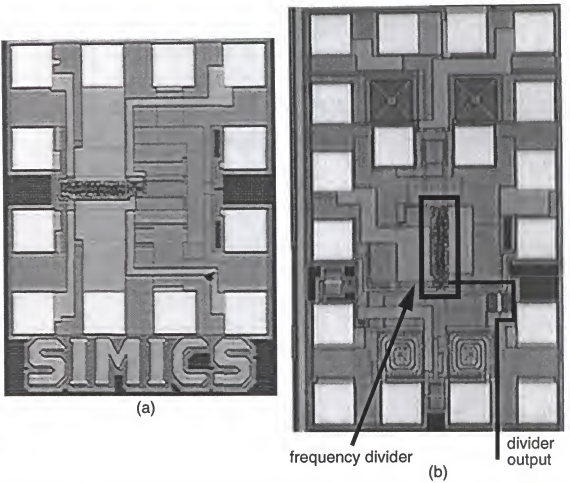


Figure 5-6 (a): A die photo of the prescaler. (b): A VCO and divider combination. The divider is right in the middle of the VCO.

The reference frequency is usually generated by a temperature compensated crystal oscillator (TCXO) and has very low phase noise (<-150 dBc/Hz @ a 20-kHz offset). The PFD is implemented with a commonly used finite (3) state machine [8]. There are two outputs (UP and DN) from the PFD. If f_{div} falls before f_{ref} falls, the signal DN is high. If f_{div} falls after f_{ref} falls, UP is high. If the falling edge of both f_{ref} and f_{div} are in phase, then both UP and DN remain low. The UP and DN signals are reset to zero when both f_{ref} and f_{div} become high while the pulse widths of UP and DN are determined by the phase differ-

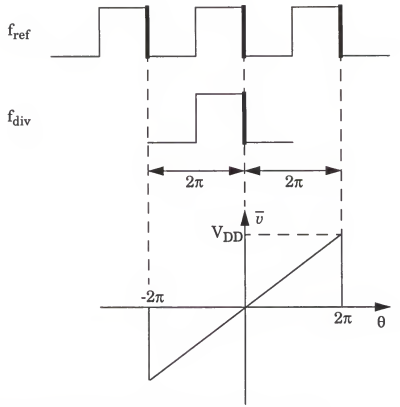


Figure 5-7 An illustration of the PFD characteristic.

ence between f_{ref} and f_{div}. The PFD can be implemented using two falling-edge triggered D-flipflops and an AND gate as shown in Figure 5-8. The operation of the PFD indicates that both f_{ref} and f_{div} must have the same frequency and phase when a PLL is locked. Since the PFD compares only the falling edges of f_{ref} and f_{div}, the difference of phase which can be detected is as large as 4π as illustrated in Figure 5-7. θ in Figure 5-7 is the phase difference between f_{ref} and f_{div}, and $\bar{v}$ is the average (over $T = 1/f_{ref}$) voltage of sum of the PFD outputs. Compared to other topologies such as a phase detector implemented using an XOR gate (which can only detect a maximum difference of 2π), the hold-in range [70] of a PLL which is defined as the frequency range for a PLL

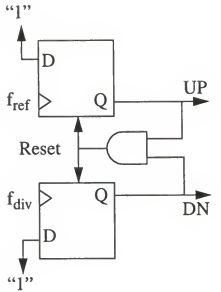


Figure 5-8 A block diagram of a phase/frequency detector.

to maintain locking can be increased using this type of PFD. Figure 5-9 shows a circuit schematic of the PFD. The circuit is symmetric between the two inputs (f_{ref} and f_{div}) as well as the two outputs. The buffers consisting of inverters at the two inputs are not included in the current design. The 2-stage inverter buffers are suggested to be inserted for future designs because f_{ref} may not be a square wave and errors would be induced when making the edge comparison by the PFD.

When f_{ref} and f_{div} are almost in phase but not perfectly in phase, suppose one of the outputs, say UP, starts to make a transition to high. However, due to a finite rise time in the PFD outputs, DN could start to go high before a full output level of UP is developed. This would reset both outputs to zero. Since the voltage levels at the two outputs are not fully developed, the PFD gain ($\bar{v}/\theta$) is reduced. If both the output voltages of PFD are not high enough to

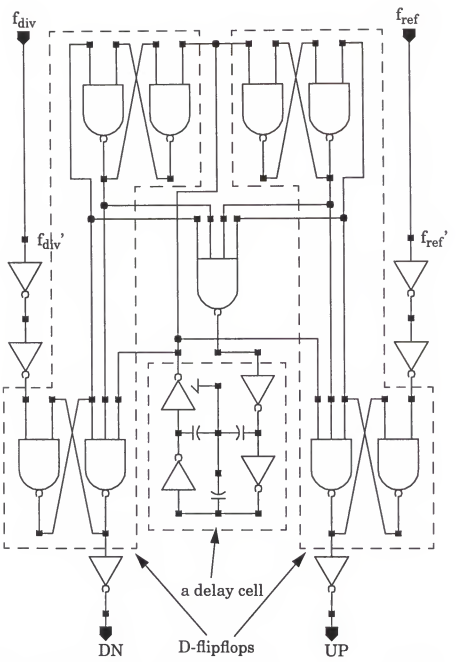


Figure 5-9 A circuit schematic of the phase/frequency detector (PFD).

turn on the switches in the charge pump, the charge pump gain and thus the PLL loop gain (section 5.2.4) becomes zero. This nonlinearity in the PFD characteristics is called a dead zone [71] in which the PLL can not properly respond to the small phase error. To eliminate the dead zone problem, a delay

cell is inserted in the PFD [72] to put off the reset signal so that UP and DN output levels can always be developed to their full level (V_{DD}). The delay cell consists of 4 stages of inverters. There are three 12-fF capacitors connected to the first 3 inverter outputs to generate the desired total delay. The total delay of ~1.3-ns is designed to guarantee that both UP and DN output levels can reach their maximum (V_{DD}). The PFD operates at ~43 MHz since the division ratio of the prescaler is 128 and the PLL output is ~5.5 GHz.

5.2.3 Charge Pump (CP)

The charge pump (CP) is controlled by the UP and DN signals generated by the PFD circuit. When UP is high, the CP deposits charges to the capacitors in the loop filter (LF) to increase the control voltage for the VCO. Similarly, when DN is high, it withdraws charges from the LF. In a conventional CP [8], the switches controlled by the UP and DN signals are directly connected between the current source transistors and the output node (Figure 5-10). Because the switches are totally turned on and off by the UP and DN signals and the voltages at drain nodes of the transistors M_1 and M_2 are V_{DD} and 0 V, respectively when the switches are off, when one of the switches is turned on, charges on either $C_{tr,up}$ or $C_{tr,dn}$ (transistor parasitic capacitances) and those on the capacitors in the LF (illustrated by a single capacitor C_{LF} in Figure 5-10) would be shared. This would induce large glitches in the CP current. The glitches would then increase the phase noise and power level of the spurs in the PLL output spectrum.

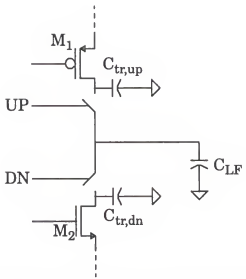


Figure 5-10 The configuration of a conventional charge pump.

A circuit schematic of the CP is shown in Figure 5-11. To alleviate the charge sharing problem, the switches M_{10} and M_{13} are connected between M_{11} and V_{DD}, and M_{12} and ground, respectively. The output node (cp_out) which is also the drain node of current source transistors, M_{11} and M_{12}, is connected to the LF. The current glitches which now occur at the sources of M_{11} and M_{12} due to switching of M_{10} and M_{13} would be attenuated at the output node. The 10-pF bypass capacitors C_1 and C_2 help to further attenuate the current glitches since they provide additional paths to ground. When the switches are being turned off and the transistors M_{11} and M_{12} are close to but not in off condition, the resistances looking in from the source nodes of M_{11} and M_{12} are high because the gate overdrive voltages (V_{GS}-V_T) are small. The time needed for the output current to become zero would be long due to large RC time constants at these two nodes. To reduce the transition time, two addi-

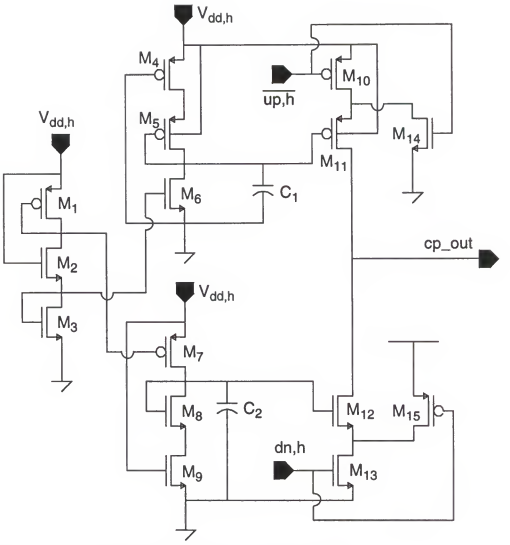


Figure 5-11 A circuit schematic of the charge pump.

tional switches M_{14} and M_{15} are connected between ground and the source of M_{11} and between V_{DD} and the source of M_{12}, respectively to provide the discharging and charging paths. Because of the additional transistors M_{10} and M_{13} connected in the current sources, M_4 and M_9 which are not included in the current design are suggested to be connected between M_5 and V_{DD}, and M_8 and ground, respectively in future designs so that the magnitude of cur-

rents in M_6 and M_7 can be accurately scaled in M_{11} and M_{12}, respectively. Otherwise, there could be mismatches between the pump up and pump down currents at the output of the charge pump which could increase power level of the spurs at the PLL output and induce a steady-state phase error between the f_{ref} and PLL output. The sizes of M_5 and M_8 are scaled down from those of M_{11} and M_{12}, respectively by ~4.5 times to reduce the power consumption in M_4-M_8. The reference current is generated on chip using M_1-M_3. The gate of M_2 is by default connected to V_{DD} and can be adjusted to vary the reference current by scratching a thin metal wire within a passivation opening. The output current of the CP is designed to be ~80 μA. The current level is chosen such that the settling time of the loop is ~14 μs with ~100-pF total capacitance in the loop filter and with $V_{DD,h}$ of ~2.7 V from the voltage doubler (section 5.2.5). The 14-μs settling time is approximated by assuming that the loop settles within a time period after the 100-pF total capacitance being charged from 0 V to V_{DD} and discharged from V_{DD} to 0 V twice (i.e. ~ $2.7 \times C_{tot} \times 4 / I_p$).

5.2.4 Loop Filter Design and the PLL Frequency Response

Because of the switching in the PLL, a charge-pump PLL is a time-varying network [73]. The simple transfer-function analysis is not directly applicable to the charge-pump PLL. However, for the frequency synthesis application, the amount of voltage changes at the charge pump output is very small in each cycle of the input signal (f_{ref}). The changes in a single

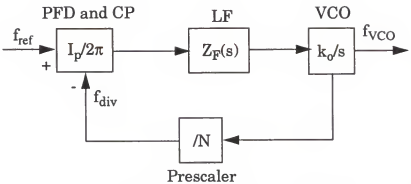


Figure 5-12 A frequency synthesizer block diagram with transfer functions of each block.

cycle becomes unimportant. Instead, the average behavior over many cycles is of relevant and the analysis using transfer functions can be applied [73].

Figure 5-12 shows a general block diagram of an integer-N frequency synthesizer with s-domain transfer functions for each block. N is the division ratio, k_o is the VCO gain (Radian/V), I_p is the charge pump current (A) and $Z_F(s)$ is the transfer function of the loop filter. The charge pump gain can be expressed as $I_p \times t_p/T / |\theta_e|$ [73] where t_p is the charge pump current pulse width due to a phase error $|\theta_e|$ between f_{div} and f_{ref} and $T=1/f_{ref}$. Since $|\theta_e| = \omega_{ref} \times t_p$, the charge pump gain becomes $I_p/2\pi$. The open loop gain (A_{OL}) of the PLL frequency synthesizer can be expressed as

$$\frac{k_o}{s} \cdot \frac{1}{N} \cdot \frac{I_p}{2\pi} \cdot Z_F(s). \tag{5.1}$$

For a charge-pump PLL, a second order filter (solid lines in Figure 5-13) is adequate [73]. The transfer function $Z_F(s)$ of the filter is

$$\frac{1 + sR_zC_z}{s(sR_zC_zC_p + C_z + C_p)} \tag{5.2}$$

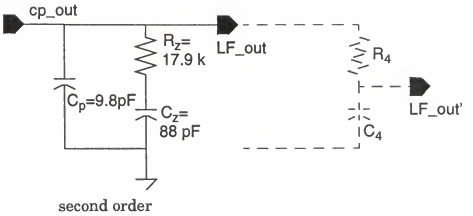


Figure 5-13 A circuit schematic of the loop filter.

Including the VCO transfer function (which is an integrator), the PLL becomes a type two, third order loop. Inserting Eq. 5.2 into Eq. 5.1, the open loop gain can be rewritten as

$$A_{OL} = \frac{k_o}{s} \cdot \frac{1}{N} \cdot \frac{I_p}{2\pi} \cdot \frac{1 + sR_zC_z}{s(sR_zC_zC_p + C_z + C_p)} \tag{5.3}$$

The zero is at $\frac{-1}{R_zC_z}$ and the poles are at 0 and $\frac{-(C_p + C_z)}{R_zC_zC_p}$. The closed-loop transfer function A_{CL} can be expressed as [11]

$$A_{CL} = \frac{A_{OL} \cdot N}{1 + A_{OL}}$$

$$= \frac{k_oI_p(1 + sR_zC_z)}{2\pi s^2[sR_zC_zC_p + C_z + C_p] + \frac{k_oI_p}{N}(1 + sR_zC_z)} \tag{5.4}$$

where the division ratio N is the inverse of the feedback gain. Due to the switching in the PLL, there would be spurs at $\omega_0 \pm f_{ref}$ where ω_0 is the PLL output frequency. Since the unity-open-loop-gain frequency ($f_{t,OL}$) is typically

much less than the reference frequency, the spurs would be suppressed by the loop. To further suppress the spurs, a third pole can be added to the loop filter as shown in Figure 5-13 (dashed lines). The output of the filter is now at LF_out' [58]. The transfer function $Z_F'(s)$ of the third order filter is

$$\frac{1+sR_zC_z}{s(sR_zC_zC_p+C_z+C_p)}\cdot\frac{1}{1+sC_4R_4} \tag{5.5}$$

The open and closed-loop gains become

$$A'_{OL}=\frac{k_o}{s}\cdot\frac{1}{N}\cdot\frac{I_p}{2\pi}\cdot\frac{1+sR_zC_z}{s(sR_zC_zC_p+C_z+C_p)}\cdot\frac{1}{1+sC_4R_4} \tag{5.6}$$

and

$$A'_{CL}=\frac{A_{OL}\cdot N}{1+A_{OL}}$$

$$=\frac{k_oI_p(1+sR_zC_z)}{2\pi s^2[sR_zC_zC_p+C_z+C_p]\cdot(1+sR_4C_4)+\frac{k_oI_p}{N}(1+sR_zC_z)}, \tag{5.7}$$

respectively.

The resistances and capacitances can be calculated by specifying $f_{t,OL}$ and the desired zero and poles. If the zero is at $f_{t,OL}/\alpha$ and the third pole is at $f_{t,OL}x\beta$, then C_p can be derived from the $\frac{-1}{R_zC_z}$ and $\frac{-(C_p+C_z)}{R_zC_zC_p}$. The required C_p is

$$C_p=\frac{k_0I_p}{2\pi N}\cdot\sqrt{\frac{1+\alpha^2}{1+\beta^2}}\cdot\frac{1}{\omega_t^2\alpha} \tag{5.8}$$

where $\omega_t=2\pi f_{t,OL}$, while C_z should be $C_p(\alpha\beta-1)$ and R_z is $\frac{\alpha}{\omega_tC_z}$. The maximum

phase of A_{OL} (Figure 5-14) occurs at $f_{t,OL} \cdot \sqrt{\beta/\alpha}$. The fourth pole can be specified at a desired frequency above the third pole, and the capacitance of C_4 and the resistance of R_4 would not change the locations of the zero and the other poles. However, the stability of the loop may become worse. To maintain an adequate stability, the minimum capacitance ratio ($\alpha\beta$-1) should be greater than 9 or $\alpha\beta$ should be greater than 10 [73]. Larger α and β result in larger C_z and better stability.

If $k_o=2\pi$ x 200 MHz/V, N=128, I_p=80 μA, the unit-open-loop-gain frequency=320 kHz and $\alpha=\beta=\sqrt{10}$ (i.e. the zero is at ~101 kHz and the third pole is at ~1.01 MHz), then R_z, C_z, and C_p can be calculated to be 17.9 kΩ, 88 pF and 9.8 pF, respectively. The Bode plots for the magnitude and phase terms of the third-order open-loop-gain using the calculated parameters are shown in Figure 5-14. The Bode plot (magnitude term) of the closed-loop transfer function (Eq. 5.4) using the same parameters is shown in Figure 5-15.

5.2.5 Voltage Doubler and Level Shift Circuits

A way to lower power consumption is to lower supply voltage. This unfortunately also reduces the voltage headroom and thus the VCO/synthesizer tuning range. To increase the VCO tuning range or range for the VCO control voltage, a voltage doubler is incorporated in the PLL synthesizer design. To reduce complexity of the voltage doubler as well as the noise in the PLL system, the number of circuit blocks driven by the voltage doubler should

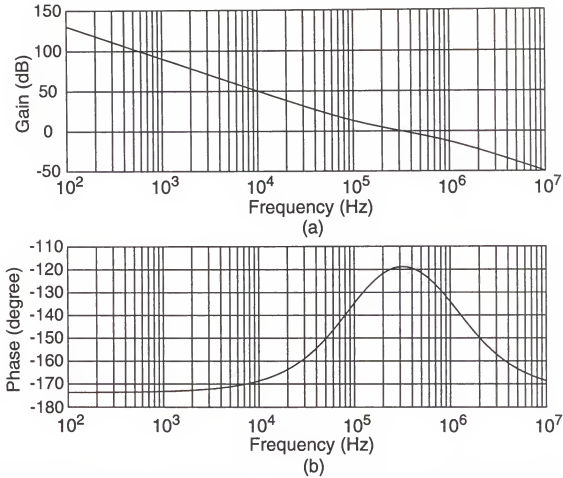


Figure 5-14 Frequency response of the open-loop gain. (a): A Bode plot of the magnitude term. (b): A Bode plot of the phase term.

be minimized and the circuits using the high supply voltage ($V_{DD,h}$) should have a good power supply rejection ratio (PSRR). Only the charge pump and interface circuit converting PFD outputs to charge pump inputs are chosen to be driven by the voltage doubler. The maximum current supplied by the voltage doubler should only be around a few hundred μA.

Because the 0.25-μm CMOS process is a 2.5-V process and the external supply voltage used for the PLL is 1.5 V, increasing the supply voltage for the charge pump to ~2.7 V should not cause reliability problems. Since the charge pump current is small, an on-chip voltage doubler [74] can be easily realized

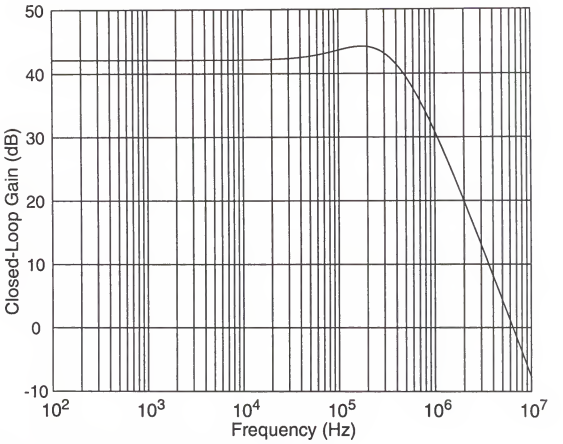


Figure 5-15 The closed-loop frequency response.

to generate the 2.7-V supply for CP. Figure 5-16 shows a circuit schematic of the voltage doubler. The voltage doubler uses the reference frequency (f_{ref}) of the PLL as the input signal. Four inverter buffers are used to drive the charge pump of the voltage doubler circuit formed by M_1 and M_2. As mentioned, V_{DD} is 1.5 V. The voltages at the sources of M_1 and M_2 are between 1.5 and 3 V and are 180° out of phase. The switches M_3 and M_4 are turned on only when their sources and gates are 3 and 1.5 V, respectively. M_5, M_6 and C_4 are used to keep the body voltages of M_3-M_6 at the output voltage of the doubler to prevent forward biasing the drain-to-body junctions of M_3-M_6. C_3 which is 100 pF

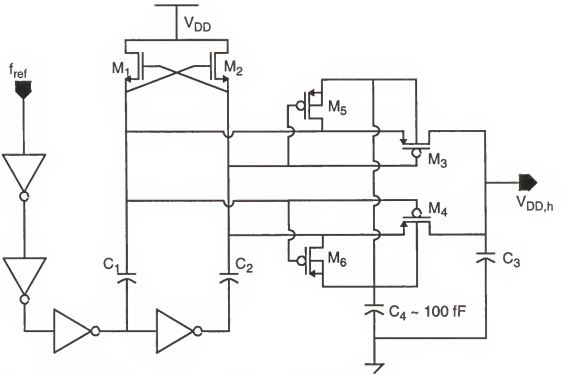


Figure 5-16 A circuit schematic of the voltage doubler.

filters the output to reduce the voltage ripple. Due to the filtering and loss of the switches as well as the loading from the CP and level shift circuits, the output dc voltage is ~2.7 V which is less than 3 V. The measured peak-to-peak voltage ripple is ~35 mV which is < 1.3% of the 2.7 V (Figure 5-17). The ripple can be further reduced with larger C_3. Due to the inductances of the dc probe and cable (i.e. ground bounce problem), the measured waveform has small ripples on the top.

The interface converting the UP and DN signals generated by PFD to the input signals up,h and dn,h of CP is designed using a level shift circuit [74]. It converts the 1.5-V square wave to a 2.7-V square wave. Figure 5-18 shows a circuit schematic of the non-inverting level-shift circuit. The inverters

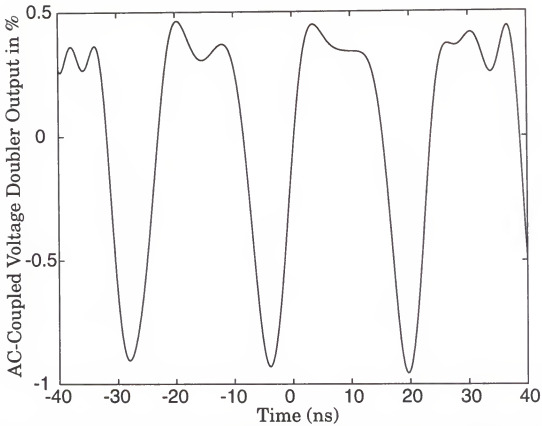


Figure 5-17 An ac-coupled voltage doubler output. The ripple is normalized to the 2.7-VDC output expressed in %.

at input use a normal 1.5-V V_{DD} while the rest of the circuit uses $V_{DD,h}$ as supply voltage. Outputs of the inverters drive the source-coupled pair formed by M_1 and M_2. The voltage difference at the drain nodes of M_1 and M_2 are then amplified by M_3 and M_4. Since M_3 and M_4 are cross-connected with positive feedback, one of their drain nodes will be pulled up to $V_{DD,h}$ while the other will be at 0 V. M_5 and M_6 form a buffer to drive the switch transistor in CP. To form an inverting level-shift circuit, gates of M_5 and M_6 can be connected to gates of M_1 and M_3, respectively. The voltage doubler can be turned off by simply disconnecting its V_{DD}.

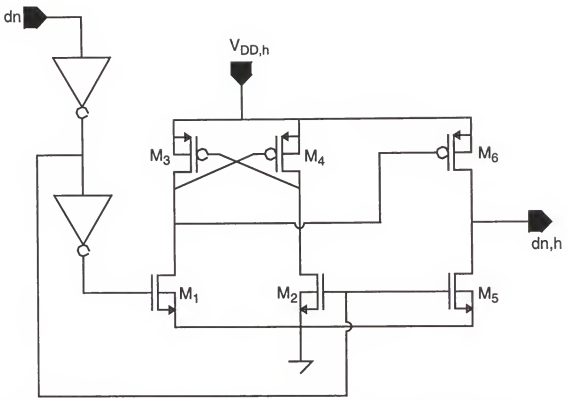


Figure 5-18 A circuit schematic of the non-inverting level-shift circuit.

5.3 Measurement Results of the Frequency Synthesizer

The PLL test structure consists of a VCO using VCO-3 with ball bonds (section 4.4.5), a divide-by-128 frequency divider (section 5.2.1), a phase/frequency detector (section 5.2.2), a charge-pump (section 5.2.3), a second-order loop filter (section 5.2.4) and a voltage doubler and level shift circuits (section 5.2.5). To enable testing of each individual block in the PLL, the PLL layout was split into 2 pad frames. Figure 5-19 shows a die photograph of the PLL test structure. The VCO and prescaler are in the top pad frame. The PFD, CP, voltage doubler, level shift circuits and loop filter are in the bottom pad frame. There are several buffers for testing individual blocks as well as for the output

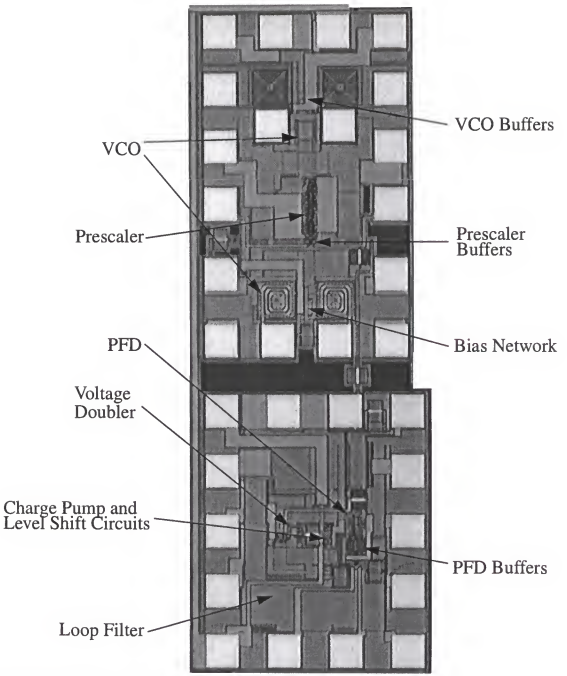


Figure 5-19 A die photograph of the PLL test structure.

of the PLL/VCO. The buffers except the one for VCO are turned off for the measurement of the close-loop PLL. The design value of the charge pump (CP) current is 80 μA, and the extracted values (from layout) of C_z, R_z and C_p in the loop filter are 79.8 pF, 13.9 kΩ and 16.2 pF, respectively. The resistance, capac-

itances and CP current are chosen such that the settling time is ~14 μs and the total capacitance is ~100 pF. The zero for the loop filter is at 143.8 kHz and the poles are located at 0 and 852.3 kHz. The unity-open-loop-gain frequency is ~258.5 kHz. However, due to a 20-pF bypass capacitor connected between VCO input control voltage and ground (for VCO characterization), the total C_p is 36.2 pF. Because of this, the actual second pole and unity-gain frequencies are 460.75 kHz and 211.4 kHz, respectively. The Bode plot (magnitude term) of the simulated closed-loop transfer function including the 20-pF bypass capacitor is shown in Figure 5-20. The peaking of the measured PLL output should be at ~200 kHz according to this simulation.

The PLL is packaged in an SOIC-like test package and the package is mounted on a low-inductance PCB board. The VCO outputs and the reference input are connected using SMA connectors. The reference input is provided using an HP8644B signal generator which has phase noise of ~-140 dBc/Hz at a 20-kHz offset. One of the PLL outputs is terminated by a 50-Ω terminator while the other is connected to an HP8563E spectrum analyzer through an external amplifier. The amplifier has a gain of ~24 dB and a noise figure of ~4 dB. The same bias condition for the VCO is applied for both open and closed-loop measurements. The phase noise of the closed-loop PLL are measured using an HP85671A phase noise measurement utility. A PLL output spectrum is shown in Figure 5-21. The reference frequency is 43.25 MHz and the PLL output frequency is 43.25x128=5536 MHz. The power level of the reference signal is 7 dBm. The PLL output power is 1.7 dBm and the resolution

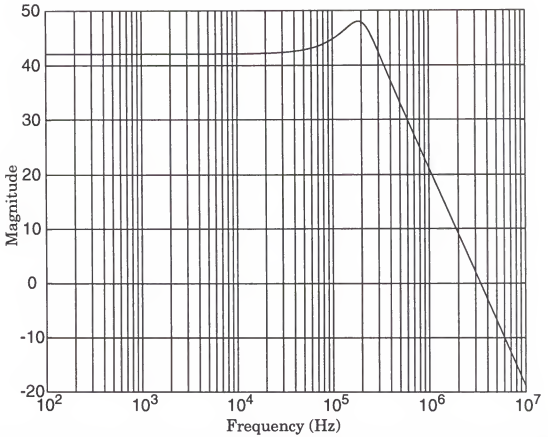


Figure 5-20 The Bode plot (magnitude term) of the actual closed-loop transfer function.

and video filter bandwidths are 10 kHz and 100 Hz, respectively. SSB phase noise plots for the free running VCO and the close-loop PLL are shown in Figure 5-22. The peaking of the PLL phase noise is at ~60 kHz which is substantially lower than the simulated (Figure 5-20). This is mainly due to the lower VCO gain at this frequency (Figure 5-23). The lower VCO gain reduces the unity-open-loop-gain frequency thus the frequency at which the magnitude of the closed-loop gain peaks (Eq. 5.8). The second reason for the bandwidth reduction is due to the utilization of MOS capacitors in the loop filter. Because the VCO control voltage is high at this frequency, the increased MOS capaci-

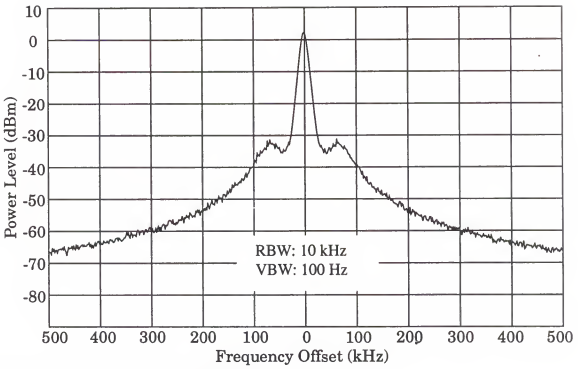


Figure 5-21 A PLL output spectrum.

tances decrease the frequencies of the zero and the third pole resulting in a smaller unity-open-loop-gain. Since the charge pump current is constant, the phase margin is decreased. The frequency-dependent loop response indicates that a circuit for linearization of the open-loop gain and phase margin is necessary. For offsets below ~30-kHz, the PLL phase noise is lower than the free running VCO noise. Extrapolating from the measurements, the PLL phase noise is >50 dB lower than that of the free-running VCO at the 1-kHz offset. The phase noise within the loop bandwidth is higher than the sum of the reference source phase noise and $10 \times \log_{10}(128^2)$ (42 dB) because the reference signal is sinusoidal and the PFD does not have an input buffer to convert the sine-wave input to a square waveform for the edge comparison (section 5.2.2). Between ~30-kHz and ~1-MHz offsets, the PLL has higher phase noise than

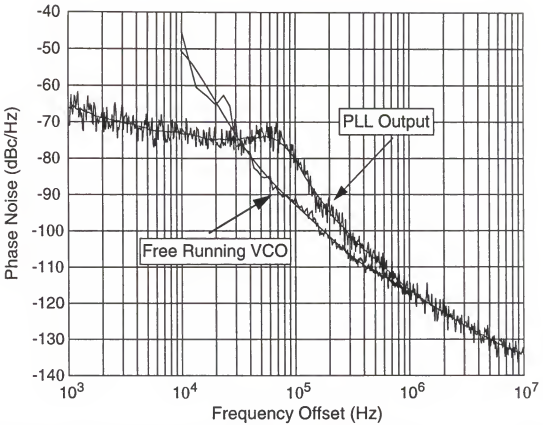


Figure 5-22 SSB phase noise plots for the free running VCO and the close-loop PLL frequency synthesizer outputs.

the free-running VCO due to the wide loop bandwidth. The PLL phase noise has a 40-dB/dec slope between ~100 and ~300-kHz offsets. This frequency dependence is from the closed-loop PLL response (Figure 5-20). If a crystal oscillator were used together with an input buffer for the PFD, and the loop bandwidth were designed to be narrower than the 60 kHz, the total PLL noise would have been smaller. The PLL frequency tuning characteristic is shown in Figure 5-23. The tuning range is ~371 MHz when the voltage doubler is enabled. The tuning range is reduced to ~301 MHz if the voltage doubler were not utilized and the charge pump were driven by a 1.5-V power supply. The VCO core and prescaler excluding the buffers for driving 50-Ω loads consume

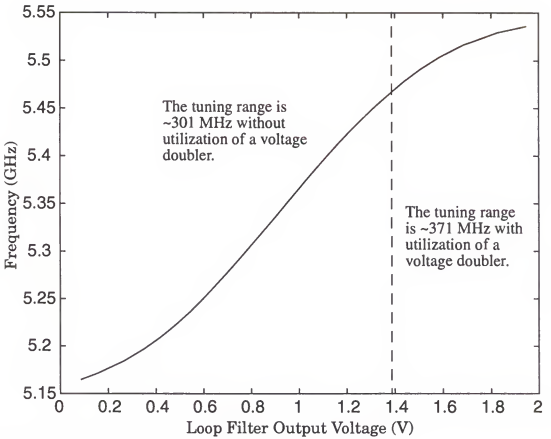


Figure 5-23 A PLL frequency tuning characteristic.

16.7 and 6.5 mW from a single 1.8-V power supply, respectively while the rest of the circuits consumes only ~1.8 mW from a single 1.5-V power supply. The 1.8-V power supply is necessary since the frequency divider does not work at 5.54 GHz with 1.5-V V_{DD}. The overall power consumption including the buffers for PLL outputs to drive 50-Ω loads is ~30.4 mW. If VCO-1 (section 4.4.3) or VCO-2 (section 4.4.4) which consumes only ~7 mW were used for the frequency synthesizer, the overall power consumption would be reduced to ~20.7 mW with similar phase noise performance.

A concern for utilizing a voltage doubler is the degradation of phase noise and the power level of spurs at the $\omega_0 \pm f_{ref}$ (since the frequency of the

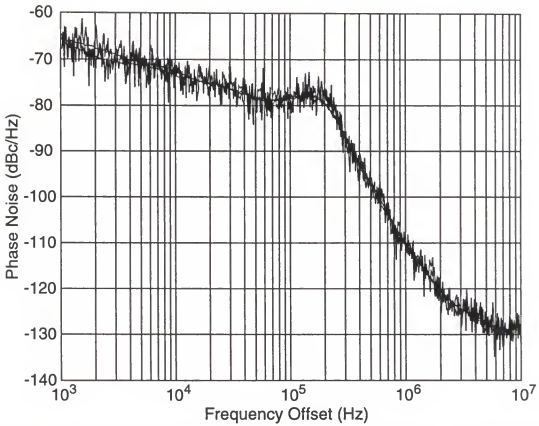


Figure 5-24 SSB phase noise plots for the PLL output with both the voltage doubler enabled and disabled.

voltage doubler input is f_{ref}). The PLL was measured both with the doubler turned on and off. The phase noise performance is essentially the same for the two cases (Figure 5-24). The power level of the spurs at $\omega_0 \pm f_{ref}$ which is dominated by the switching of the charge pump is essentially the same. The spurs are ~63 dB below the carrier. If a third-order loop filter were used, the spurs would have been even smaller. Hence, the utilization of a voltage doubler increases the PLL frequency range without significantly degrading the noise performance nor increasing the power level of spurs.

5.4 Layout Considerations

The PLL is fabricated on a high-resistivity (~8 Ω-cm) substrate. The major concern for integrating a frequency synthesizer on a single chip is the noise coupling to a VCO from a prescaler. As mentioned in CHAPTER 4, there should not be any closed loop surrounding the inductors. Especially in a PLL which forms a loop, care must be exercised to break any loops formed by the interconnects as well as capacitors (section 4.4.5). The prescaler which is typically near the VCO can inject large switching noise into the substrate. The noise can be coupled back to the VCO degrading the spectral purity of the VCO. However, as demonstrated in section 5.2.1, the prescaler designed for this PLL is quiet and it is possible to integrated both. Adding a large amount of substrate contacts surrounding the prescaler to ground the switching noise generated by the prescaler, and minimizing the coupling and parasitic capacitance among routing wires (such as those between the outputs of the VCO and prescaler) in the layout should be sufficient.

In addition to the VCO and prescaler, the phase/frequency detector, charge pump, voltage doubler and loop filter in the frequency synthesizer are digital or mixed-mode circuits. Good shielding and isolation are required to protect the sensitive VCO from the noise coupling. Ground-shielded pads and large-area substrate contacts are used all over the PLL layout to reduce the substrate coupling. The V_{DD}s for the VCO, prescaler and the rest of the PLL are also separated to reduce the coupling through the power lines.

5.5 Summary

As demonstrated in section 5.2.1, a 5.4-GHz frequency divider operating at V_{DD}=1.5 V has been successfully developed using a 0.25-μm digital CMOS process. However, it does not have any margin and currently limits the maximum operating frequency of the synthesizer. This will be especially true when the required dual-modulus prescaler is implemented in a 0.25-μm process. The divider has low switching noise and low power consumption. The self-oscillation characteristic as well as the advantages and disadvantages of the source-coupled logic structure were qualitatively examined. The SCL structure is capable of low-voltage, low-power-consumption, low-switching-noise and high-frequency operation. At 5.4 GHz, the prescaler consumes only 4.1 mW from a 1.5-V V_{DD}. The maximum operating frequency can be increased with larger power consumption. Even when the prescaler is integrated within the VCO layout, the effects of the prescaler switching noise to the VCO phase noise performance and VCO output spectrum at $f_{VCO} \pm f_{div}$ (f_{VCO}/128) are small.

The charge pump is designed to reduce the current glitches at the output by moving the switch transistors away from the output node. The low current glitch should reduce the power level of spurs at $\omega_0 \pm f_{ref}$. Two additional transistors are added to reduce the rise and fall time of the current pulses. A voltage doubler which uses the reference signal of the PLL and an 1.5-V power supply as inputs generates a 2.7-V output. Level shift circuits are also

designed to convert the 1.5-V PFD outputs to 2.7-V inputs for the charge pump. Using the voltage doubler to drive the charge pump, the input voltage (control voltage) range of the VCO can be extended from between ~0.12 and ~1.4 V to between ~0.12 and ~2.6 V thus increasing the VCO/PLL frequency tuning range from 301 to 371 MHz. The ~35-mV ripple at the 2.7-V voltage doubler output has minor impact to the PLL phase noise and the spurs in the PLL output spectrum.

A frequency synthesizer using the VCO-3 is demonstrated. The phase noise within the loop bandwidth is ~-75 dBc/Hz at a 20-kHz offset. This phase noise performance is about average due to the sinusoidal reference input signal and the high phase noise of the reference source (compared to a low-phase-noise crystal oscillator). The spurs at $\omega_0 \pm f_{ref}$ are 63 dB below the carrier. If a third-order loop filter were used, the spurs would have been even smaller. The total power consumption of the PLL is 30.4 mW from a 1.8-V supply for the VCO and prescaler and a 1.5-V supply for the rest of the loop components. If the other integrated 5-GHz VCOs (from CHAPTER 4) were used in the PLL, the PLL power consumption would have been reduced to ~20.7 mW while maintaining the same phase noise performance. These results suggest that using a 0.25-μm CMOS process, integration of low-cost and low-power frequency synthesizers for high bit-rate applications at 5 GHz is feasible.

CHAPTER 6
SUMMARY AND FUTURE WORK

6.1 Summary

The requirements of frequency synthesizers for modern communication systems are rigorous which make it difficult to integrate a single-chip radio consisting of a frequency synthesizer and other functions using a low-cost CMOS process. A key for implementing high-performance RF circuits is the high-quality-factor passive components. Methodologies for design and optimization of MOS capacitors, pn-junction varactors and transistor parasitic capacitances have been developed. The guidelines for inductor design have also been summarized. Quality factors of >140 at 5.5 GHz and >40 at 26 GHz for MOS capacitors have been demonstrated in a 0.25 and a 0.1-μm CMOS processes, respectively. The n-well-to-p-substrate parasitic capacitance in an MOS capacitor does raise a concern for linearity when the MOS capacitor is connected in series. However, using the capacitors, low-noise amplifiers (LNAs) with P_{1dB} and P_{IP3} sufficient for many applications have been demonstrated [31], [75] suggesting that the linearity of an MOS capacitor is adequate. In addition to the MOS capacitor, Q of 57 at 5.5 GHz for a pn-junction varactor has also been achieved. These results provided a foundation for developing low-phase-noise voltage-controlled oscillators (VCOs) and circuit

blocks needed for an integrated frequency synthesizer. Passive components fabricated in a p^+ and a p^- substrates were compared in a 0.25-μm CMOS process. The inductor Q which typically dominates the overall Q of an on-chip LC network is significantly higher in a p^- substrate which makes p^- substrates preferable.

The phase noise of a frequency synthesizer outside the loop bandwidth is mainly determined by the VCO. Using a modified negative-g_m circuit topology with only PMOS transistors in the VCO core and the high-Q passive components, fully integrated VCOs as well as VCOs using a combination of on-chip spiral inductors and package parasitics at 1-GHz and 5-GHz frequency bands have been fabricated using standard digital CMOS processes. The measured phase noise is the lowest reported compared to those of previously published in the literatures. The frequency tuning range and power consumption are reasonable. A bias network is also integrated within the 5-GHz VCOs to increase the power supply rejection ratio. A relaxation oscillator operating at ~10 GHz and an LC oscillator operating at ~26 GHz have also been demonstrated. The 26-GHz VCO is the CMOS circuit with the highest operating frequency ever reported. It also suggests that CMOS circuits operating at >30 GHz is possible.

The second challenging circuit block in a frequency synthesizer is the frequency divider which is required to be low-noise, to have low power consumption and to be able to operate at the VCO output frequency. A prescaler which uses an SCL structure, and has low switching noise and low power con-

sumption has been demonstrated. When integrated with a VCO, the effects of the noise generated by the prescaler to the VCO phase noise performance and VCO output spectrum at nf_{div} (where $f_{div}=f_{vco}/128$ is the divider output frequency and n is an integer) are immeasurable. The experimental results indicate that the prescaler is suitable for the PLL applications.

A new charge pump with low current glitches at its output node, and short rise and fall time for the output current pulses has been designed and fabricated. Using an on-chip voltage doubler and level shift circuits, the output voltage of the charge pump has been increased to ~2.6 V in order to increase the VCO tuning range. Together with a low-phase-noise VCO, a frequency divider and a phase/frequency detector, a low-cost integrated PLL frequency synthesizer operating at 5.5 GHz with low phase noise and low power consumption is demonstrated. The spurs are 63 dB below the carrier. The experiences gained by completion of this work provide insights into the flexibility and capabilities of CMOS technologies for implementing an RF front end at 6 GHz and beyond, and have contributed toward the implementation of a CMOS single-chip radio in the future.

6.2 Future Work

This work has answered many questions. But in the process, it has also raise many questions and concerns, and brought other possibilities to forefront which need further attention. These include:

1. High quality factors for the passive components have been achieved. However, to increase the frequency tuning range of a VCO to cover the temperature and process variations, the capacitance range of the MOS and pn-junction varactors needs to be improved. Especially for a deep-submicron CMOS process, the capacitance range becomes smaller due to a larger capacitance contribution from the overlap and fringing capacitances. The polysilicon gate depletion effect further decreases the usable capacitance range. A systematic method to find out the optimal gate dimensions for a given frequency and process should be established. A variation of the MOS capacitor structure may be developed to widen the capacitance range.
2. It has been shown that cascaded LC oscillators may have lower phase noise [76]. However, the power consumption is much higher than a single stage LC oscillator. Using a modified circuit topology presented in CHAPTER 4 and having multiple resonators in a single stage VCO, the power consumption may be significantly improved while achieving similar or better phase noise performance compared to [76].
3. At low frequencies, it is easier for a capacitor to achieve high quality factor while it is more difficult for an inductor. The situation is reversed at high frequencies. There should be an optimal frequency f_{opt} for a VCO to have the best phase noise performance using a given process technology. Using the VCO operating at f_{opt}, other desired frequencies may be generated using frequency synthesizers and/or frequency divid-

ers. Of course, a fractional-N frequency synthesizer architecture may be needed to have the required frequency resolution. Development of such a system is recommended to further improve the phase noise performance.

4. Using the 0.1-μm CMOS process, it should be possible to implement VCOs operating at higher frequency than 26 GHz. The limit for the maximum VCO frequency in CMOS technologies should be investigated.

APPENDIX A

DERIVATION OF THE SPREADING EFFECT USING A DISTRIBUTED MODEL

Figure A-1 illustrates a distributed model used for the MOS capacitor. R and C are the total resistance and capacitance, respectively from the layout geometry while r=R/l and c=C/l are the resistance and capacitance per unit length, respectively in the distributed model, where l is the length of the transmission line (Figure A-1). Using s-domain expressions, the nodal equations using Kirchhoff's current and voltage laws are

$$I(x) - \frac{V(x+\Delta x)}{\frac{1}{sc\Delta x}} = I(x+\Delta x)$$
$$\Leftrightarrow \frac{dI(x)}{dx} = V(x) \cdot sc \qquad \text{(A.1)}$$

and

$$V(x) - I(x) \cdot r \cdot \Delta x = V(x+\Delta x)$$
$$\Leftrightarrow \frac{dV(x)}{dx} = I(x) \cdot r$$

Combining Eqs. A.1 and A.2 yields

$$\frac{d^2 I(x)}{dx^2} = scrI(x) \qquad \text{(A.3)}$$

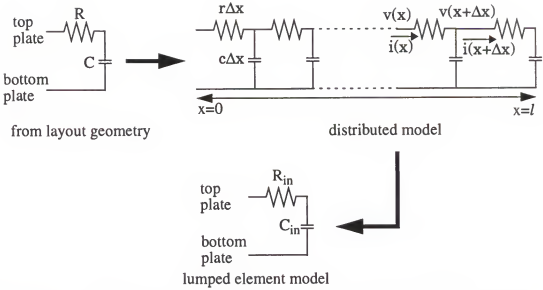


Figure A-1 An illustration of the distributed model for an MOS capacitor.

and

$$\frac{d^2V(x)}{dx^2} = scrV(x) \tag{A.4}$$

Let γ^2=scr and Z_0=γ/sc, the solution to Eqs. A.3 and A.4 is

$$V(x) = V_0^+ e^{-\gamma x} + V_0^- e^{\gamma x} \tag{A.5}$$

$$I(x) = I_0^+ e^{-\gamma x} + I_0^- e^{\gamma x} = \frac{V^+_0}{Z_0} e^{-\gamma x} - \frac{V^-_0}{Z_0} e^{\gamma x} \tag{A.6}$$

where V^+_0 and V^-_0 are voltage amplitudes, I^+_0 and I^-_0 are current amplitudes, and $e^{-\gamma x}$ and $e^{\gamma x}$ represent the outgoing and incoming waves, respectively [35]. Using Eq. A.6 and the boundary condition $I(l)=0$ yields $V^+_0=V^-_0\, e^{2\gamma x}$. The input

impedance Z_{in}

$$Z_{in} = \frac{V(0)}{I(0)} = \frac{V_0^+ + V_0^-}{\frac{V^+0}{Z_0} - \frac{V^-0}{Z_0}} = Z_0 \cdot \frac{V^-0 e^{2\gamma l} + V^-0}{V^-0 e^{2\gamma l} - V^-0} = Z_0 \cdot \coth\gamma l = \frac{\gamma}{sc} \cdot \coth\gamma l \quad \text{(A.7)}$$

Since $\gamma l = \sqrt{scrl^2} = \sqrt{sCR}$ is small (<0.01 at 1 GHz) for the ~150-fF MOS capacitor test structure, $\coth\gamma l$ can be approximated as

$$\coth\gamma l = \frac{1 + \frac{(\gamma l)^2}{3}}{\gamma l} \quad \text{(A.8)}$$

Substituting Eq. A.8 into Eq. A.7, Z_{in} becomes

$$Z_{in} = \frac{\gamma}{sc} \cdot \frac{1 + \frac{(\gamma l)^2}{3}}{\gamma l} = \frac{1}{sC} + \frac{1}{3} \cdot \frac{scrl}{sc} = \frac{1}{sC} + \frac{R}{3}$$

Hence, the equivalent input resistance R_{in} is reduced to R/3 while the input capacitance C_{in} remains the same as C.

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